Courant Institute of

Mathematical Sciences

AEC Computing and Applied Mathematics Center

A 16 Channel Medium Speed Multiplexer

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1. INTRODUCTION

A medium speed multiplexer system that interfaces 16 synchronous serial channels to a Honeywell 16-bit series computer is described in this report. The system permits simultaneous communication between the Control Data 6600 computer, at the Courant Institute of Mathematical Sciences, and any 16 sites accessible by telephone or private line.

The salient features of the system are:

a. The multiplexer channels function with any synchronous data device in a half or full duplex mode.

b. The multiplexer channels handle data rates up to 10k bps.

c. The multiplexer channels are individually synchronized by the data channel clocks.

d. Eight-bit byte registration for a channel in the input mode is accomplished within the multiplexer. This feature can be bypassed for any channel if complete data transparency is desired.

e. Software overhead is less for 16 channel communication with the multiplexer/computer composite than with the computer alone and attendant interfaces.

f. The operating modes of each channel are controlled by the Honeywell computer software.

g. The data passing through the multiplexer, whether trans-
mitting or receiving on any channel, is in no way alter-
ed. The philosophy of data transparency, a necessity in
a research environment, is thus adhered to.

The multiplexer handles all remote batch entry of the CDC-6600.
Figure 1 shows the CDC-6600/DDP-516 configuration[*] at the Computing
Center.

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[*]The CDC-6600/DDP-516 interface and the remote entry system
for the CDC-6600 are described in the following AEC Research and
Development Reports published by New York University: Bianchini,
R. P., "An Interface Between a Control Data 6600 Series Computer
and a Honeywell 16-Bit Series Computer", NYO-1480-119, October
1969; Francheschini, E., Feinroth, Y., and Goldstein, M., "A
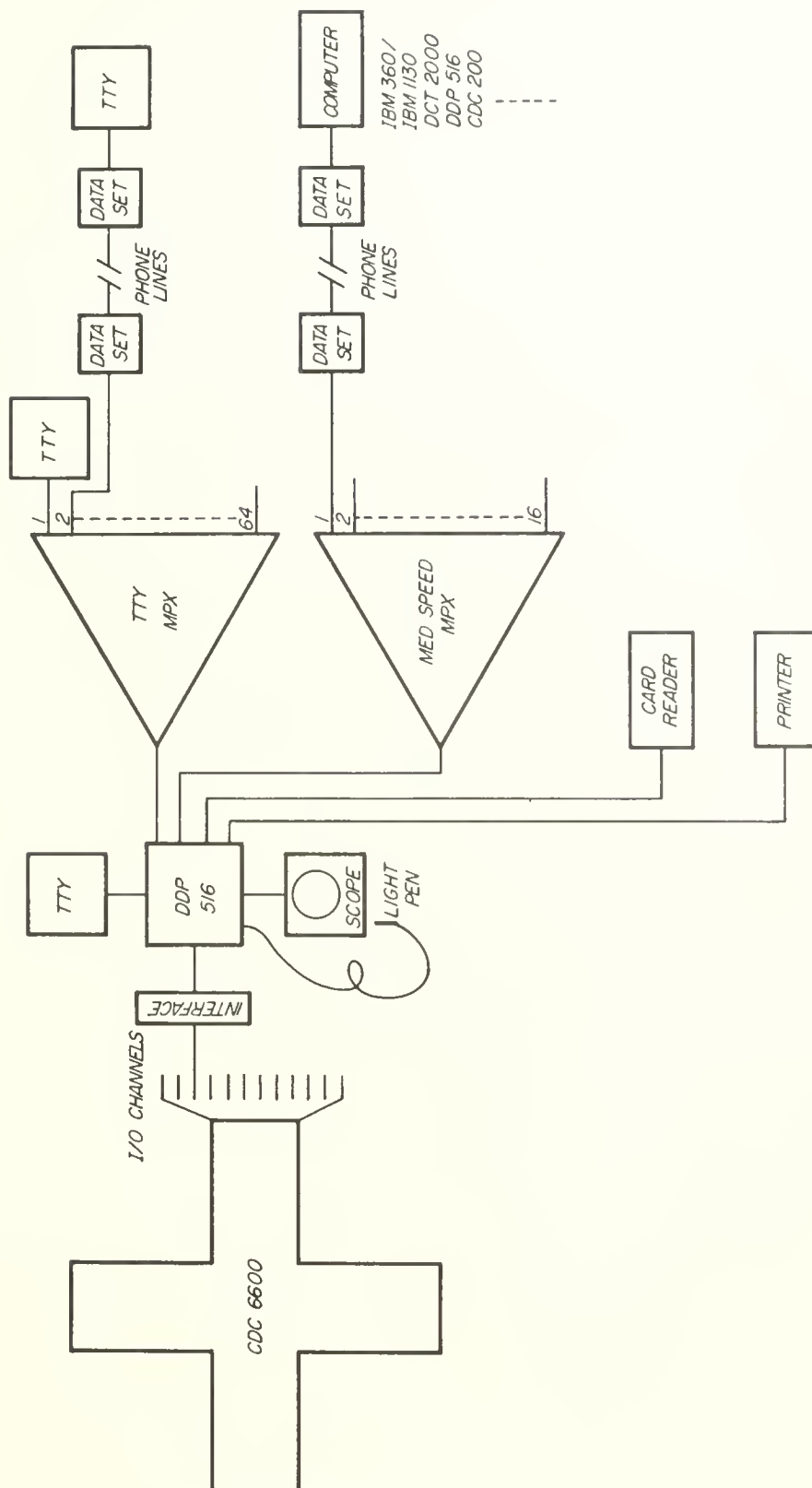Remote Entry System for the CDC-6600", NYO-1480-148, April 1970.

FIGURE 1 — 6600/516 CONFIGURATION

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2. SYSTEM OPERATION

The remote entry configuration of the CDC-6600 consists of 16 synchronous serial channels interfaced by the multiplexer to a Honeywell 16-bit computer. The Honeywell computer is interfaced to the CDC-6600. This small "front end" computer, which is interfaced to the CDC-6600, performs the dual function of I/O controller and temporary storage. Any of the Honeywell models DDP-116/416/516 or H-316 can be used for this purpose.

The data to and from the serial channels is in the form of bit streams driven by channel clocks. The I/O structure of the Honeywell computer permits communication on a byte level. Therefore, the throughput of the multiplexer requires that it contain a memory. Since the multiplexer/computer communication is asynchronous, the multiplexer must be capable of communicating to the computer the real time requirements of the 16 serial channels. Accordingly, the multiplexer utilizes the hardware interrupt feature of the computer.

From an overall system point of view, the computer outputs data through the multiplexer to any one of the 16 serial channels. Transmission from computer to multiplexer is in 8-bit bytes. The multiplexer distributes the bytes as specified by the computer. Then the 8-bit bytes are marched out serially onto the appropriate channels. Since the channels are synchronized to channel trans-

mission clocks, the computer must maintain an output data rate of one 8-bit byte for every 8 counts of the corresponding channel transmission clock.

The computer collects data from any one of the 16 serial channels. The bit streams are synchronized to channel derived receive clocks. The multiplexer collects and stores the bits into groups of 8-bit bytes. The computer takes these bytes along with additional information for channel identification. Since the channels are synchronized to channel derived receive clocks, the computer must maintain an input data rate of one 8-bit byte for every 8 counts of the corresponding channel clock. While the bits are collected, the multiplexer hardware establishes the byte synchronization of the received message. The computer software is thus relieved of this task. A hardware switch can bypass this feature for any channel.

The multiplexer allows each of the 16 channels to operate independently. Thus, each channel may operate in a receive or transmit mode, at different data rates, in full or half-duplex, and with or without byte synchronization for received messages.

The computer interrupt circuitry controls the byte level communication between the computer and multiplexer. When the computer is interrupted for input, it collects the 8-bit bytes that the receive channels have ready. When the computer is interrupted for output, it outputs the 8-bit bytes that the multiplexer can accept for the channels in the transmit mode.

The multiplexer memory contains 48 bits for each channel: 24 for input and 24 for output data. In each case, double level byte buffering is employed. The design allows the computer an 8 bit time interval for servicing the multiplexer for input or output data. A real time hardware clock in the multiplexer paces the computer input and output interrupts. The real time bit requirements of the 16 serial channels determine the pacing rate.

Previous techniques would have required the computer to treat the 16 serial channels with individual 8-bit byte interfaces as separate devices, all with separate interrupts. This creates a software environment with a high interrupt overhead. The multiplexer has only two interrupts for all of the 16 serial channels: one for input, one for output. This feature reduces the interrupt software overhead that is required for communication between the 16 serial channels and the computer.

3. HARDWARE STRUCTURE

The multiplexer comprises four sections--see Fig. 2.

A. Clock, Timing, and Decode Circuitry. Synchronizes the delay line memory to the pre-multiplexer scanning and to the computer/multiplexer interface.

B. Pre-Multiplexer. Synchronizes each serial data channel to the multiplexer memory. Contains the individual channel mode selection switches.

C. Delay Line Memory. Consists of twelve 1 MHz delay lines for double level buffering of each of 16 channels. Each delay line has a 64 bit capacity.

D. Computer/Multiplexer Interface. Functions as a communication channel between the delay line memory and the computer. Can buffer an 8-bit byte for computer input and output data. Buffering is necessary because of the 64 μsec access time of the delay line memory.
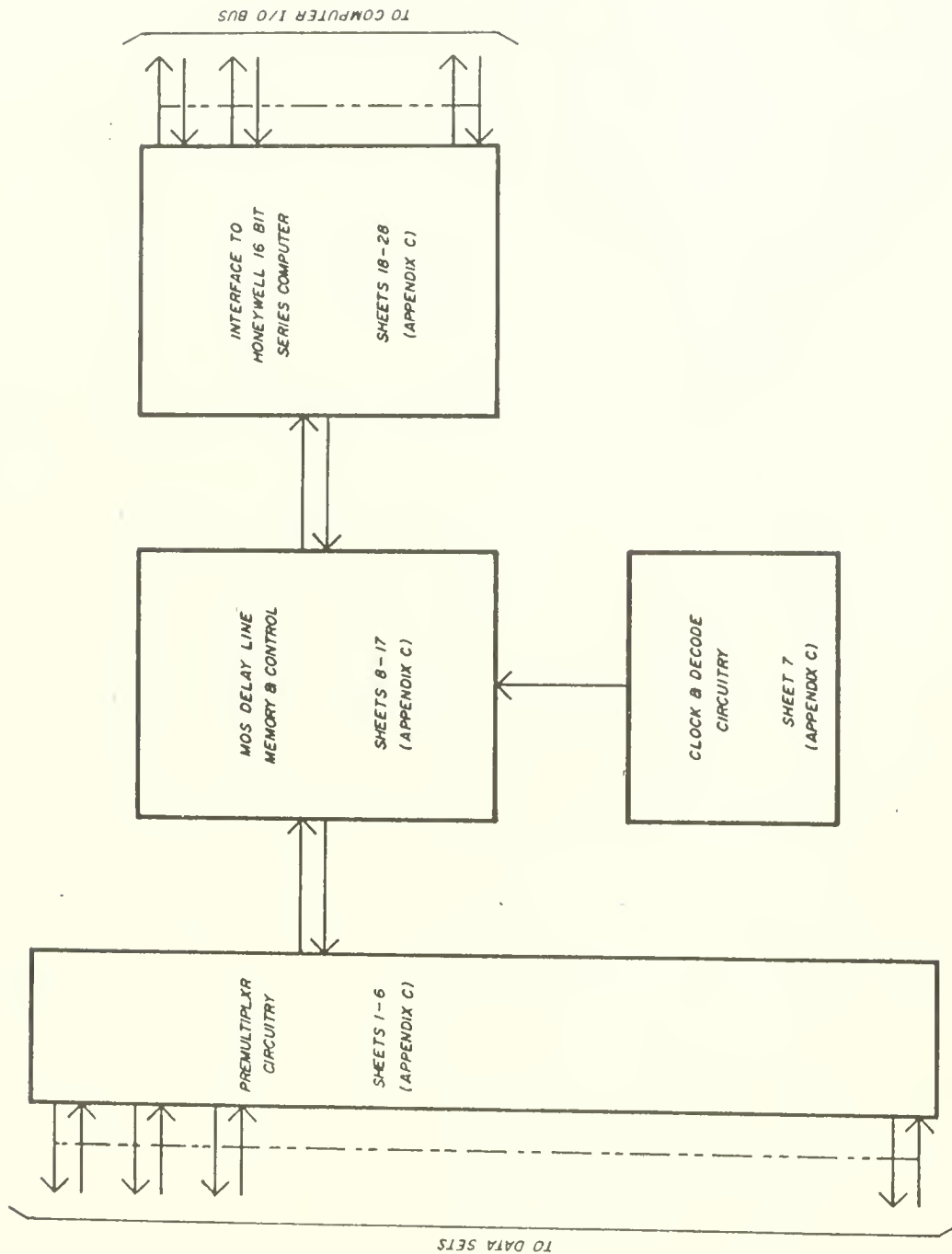
FIGURE 2 - SYSTEM BLOCK DIAGRAM OF 16 CHANNEL MULTIPLEXER

TO COMPUTER I/O BUS

INTERFACE TO
HONEYWELL 16 BIT
SERIES COMPUTER

SHEETS 18-28
(APPENDIX C)

MOS DELAY LINE
MEMORY & CONTROL

SHEETS 8-17
(APPENDIX C)

CLOCK & DECODE
CIRCUITRY

SHEET 7
(APPENDIX C)

PREMULTIPLXR
CIRCUITRY

SHEETS 1-6
(APPENDIX C)

TO DATA SETS

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3A. Clock, Timing, and Decode Circuitry

(See Appendix C Schematics, Sheet no. 7)

Contains a 1 MHz crystal control clock, a 6 bit countdown chain, a 2 bit decoder, and a 4 bit decoder. The 2 bit decoder cycles every 4 clock counts; the 4 bit decoder cycles every 64 clock counts. See Fig. 3. Since the 1 MHz clock drives the delay lines, one cycle of the 4 bit decoder corresponds to one delay line trip. Fig. 4 shows the timing relationship of all the clock outputs. The 4 bit decoder has sixteen 4 μsec states: 00_8, 01_8, 02_8, 03_8,...17_8. Each state has four 1 μsec sub-states: T0, T1, T2, and T3. Thus in the sequential time allocation of the 16 data set channels, the time slice for each is subdivided into four 1 μsec sub-states: T0, T1, T2, and T3.
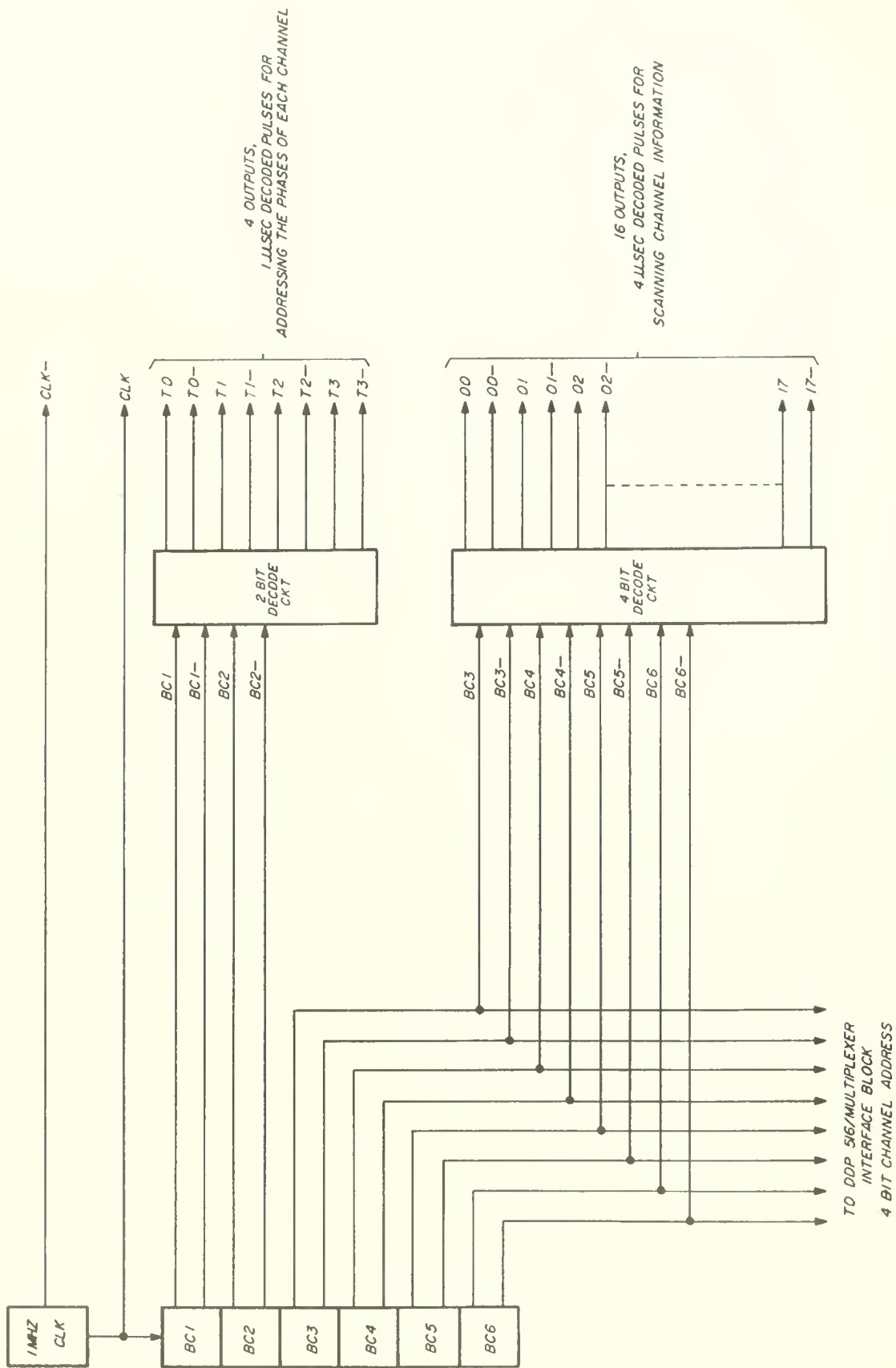
FIGURE 3 – SYSTEM CLOCK AND DECODE *CIRCUITRY*

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TIMING WAVESHAPES GENERATED BY CLK, DEC CIRCUITRY

FIGURE 4

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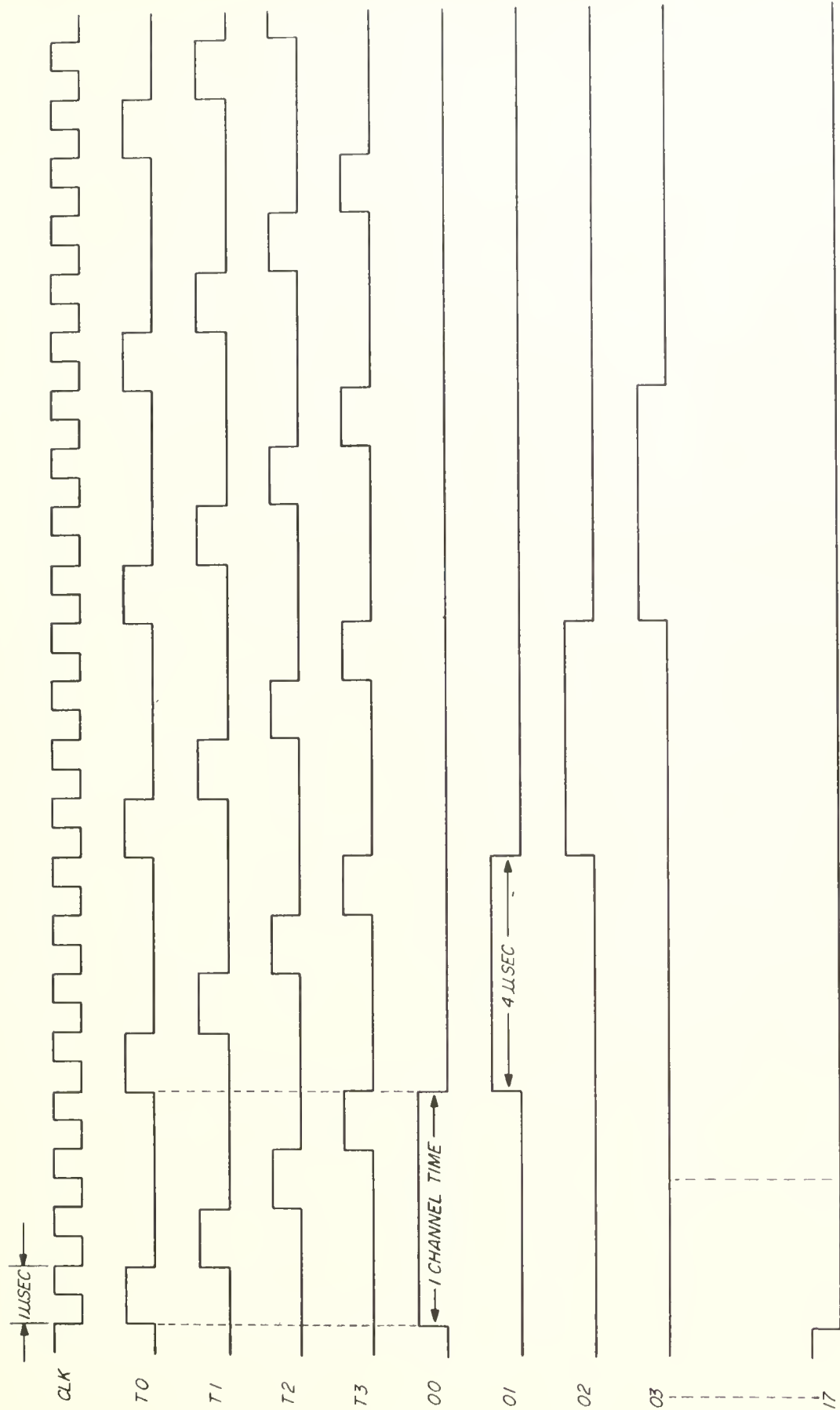
3B. Pre-Multiplexer Circuitry

(Appendix C Schematics, Sheets 1-6)

Each pre-multiplexer channel comprises seven flip-flops, "nand" gates for scanning and control, and level convertor circuits for voltage compatability between the pre-multiplexer and the synchronous serial data channels.

Two flip-flops are used for channel mode selection, and are separately controlled by the computer software. Two flip-flops are used for receiving serial data from the channel. Three flip-flops are used for transmitting serial data onto the channel.

Data Terminal Ready Flip-Flop

In the "1" state, enables the channel to operate. In the "0" state, closes off the logic and disconnects the channel from the remote user.

Request to Send Flip-Flop

In the "1" state, sets the channel into the transmit mode. In the "0" state, sets the channel into the receive mode. The state of this flip-flop is forced by a hardware switch when the channel is used in a full-duplex mode.

Receive Data and Receive Clock Flip-Flops

The receive data flip-flop functions as a one-bit serial buffer. The receive clock flip-flop functions as a switch which is set by the channel receive clock. The switch remains set until the delay line memory can accept the bit from the receive data flip-flop. This can occur only during the 4 μsec time slice assigned to the channel.

Transmit Clock and Two Transmit Data Flip-Flops

The transmit clock flip-flop functions as a switch which is set by the channel transmit clock. The switch remains set until the delay line memory can output data to the two transmit data flip-flops. The two flip-flops function as a two bit serial buffer which outputs data to the channel at a rate determined by the transmit clock.

3C. Delay Line Memory

(Appendix C Schematics, Sheets 8-17)

This section of the hardware contains the memory required for control and double level buffering of all of the 16 serial data channels. The receive buffers are used with a compare circuit to establish byte synchronization of the receive message. The memory consists of 64 sequential 12-bit words. A new word is accessed from the sequential memory at a 1-µsec rate. The total cycling time of the memory is 64 µseconds. Four of the 12-bit words are used for handling data bits of each serial data channel.

Channel bit storage requirements are shown in Tables I and II, p. 17-19. Delay line memory bit assignments are shown in Fig. 5. The first two words, T0 and T1, are used for channel receive data. The second two words, T2 and T3, are used for channel transmit data. Because of the sequential nature of the memory, byte transfers from T0 to T1 and T2 to T3 are accomplished by using an 8-bit data delay register (8 flip-flops). Accordingly, in the receive mode, the channel data collection buffer T0 precedes the byte static buffer T1; in the transmit mode, the channel data distribution buffer T3 follows the static buffer T2.

The combination of serial and parallel 8-bit buffers, for input and output, forms the double level buffering mechanism for each channel. The byte static buffers store 8-bit bytes. The serial

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buffers satisfy the real time requirements of the serial data channels (one bit per channel clock interval).

The delay line memory consists of the following circuitry plus interconnecting logic and flip-flops--see Fig. 6.

8-Bit Data Register

This register is inserted between the output and input of the delay line memory. It is used to transfer byte data from the serial buffer to the byte static buffer (receive mode), or from the byte static buffer to the serial buffer (transmit mode). These transfers take place when the input serial buffer goes full, or when the output serial buffer goes empty.

Synch Compare Circuitry

Establishes the first bit of a receive message. The circuit compares the contents of the receive serial buffer against a known pattern (synch), as the receive bit stream is marching through the receive serial buffer.

Add "1" Logic

Six bits for each channel are reserved in memory to store two separate 3 bit counts. One set is for the number of receive serial buffer shifts, the other is for the number of transmit serial buffer shifts. The add "1" logic updates these counters every time data is shifted.

Twelve 64-Bit Delay Lines

Each delay line is a 64-bit MOS 1 MHz shift register. A stored bit can only be read when it is shifted out of the end of the delay line. By feeding the delay line output back into the input logic gates, a bit can either be stored indefinitely or modified as required. An expandable "or" node is provided at the input of each delay line. This allows for the addition of as many control functions as needed. The 12 delay lines operate in parallel; therefore, at any one time, a 12-bit word is read out by looking at the output of each of the delay lines. Because of the output to input feedback, this word can be either stored indefinitely or modified. When clocking these lines at a 1 MHz rate, a new 12-bit word appears at the outputs of the delay lines every one μsecond. Since these lines are 64 bits long, a particular 12-bit word is accessible every 64 μseconds. At this point, it can either be modified or reinserted as is into the lines. The lines operate in complete synchronism with the scanning of the 16 pre-multiplexer channels. Each pre-multiplexer is allowed a 4 μsec time slice--Fig. 7. During this time slice 4 sequential, 1 μsec 12-bit words of delay line memory are accessible. This occurs for each pre-multiplexer channel every 64 μseconds.

Table I - Input Data Bits For Each Serial Channel

1. 7 bits are used as a serially loaded, parallel-out shift register buffer. The buffer shifts in data at a rate equal to the receive channel clock.

2. 8 bits are used as a parallel-in, parallel-out byte static buffer.

3. 3 bits are used to store the number of shifts of the receive serially loaded buffer. The count is updated by 1 for each shift of the serial buffer.

4. Full bit. This is a switch which is set when the serial buffer is full, and its contents are transferred to the static buffer. This occurs when the 3-bit stored count cycles through its zero state. The switch is reset when the multiplexer/computer interface can accept the 8-bit byte from the byte static buffer.

5. 2 bits are used to establish the first bit of the receive message. These are the pre-synch and synch bits.

6. 2 bits are used to mark the first bit of the receive message, and to send a termination word to the computer when the serial

channel is no longer receiving data. These are the start and
stop bits.

7. Overwrite bit. This is a switch which is set when the com-
    puter fails to meet the receive real time byte requirements
    of the serial channel.

Table II - Output Data Bits For Each Serial Channel

1. 8 bits are used as a parallel-in, parallel-out byte buffer.

2. 8 bits are used as a parallel-in, serial output shift reg-
    ister. This buffer shifts out data at a rate equal to the
    transmit channel clock.

3. 3 bits are used to store the number of shifts of the transmit
    serial output buffer. The count is updated by 1 for each
    shift.

4. Empty bit. This is a switch which is set when the serial out-
    put buffer is empty. At this point, an 8-bit byte is trans-
    ferred to it from the byte static buffer. This occurs when
    the 3-bit stored count cycles through its zero state. The
    switch is reset when the multiplexer/computer interface loads
    the static buffer with another 8-bit byte.

5. Underwrite bit. This is a switch which is set when the com-
    puter fails to meet the transmit real time byte requirement
    of the serial channel.
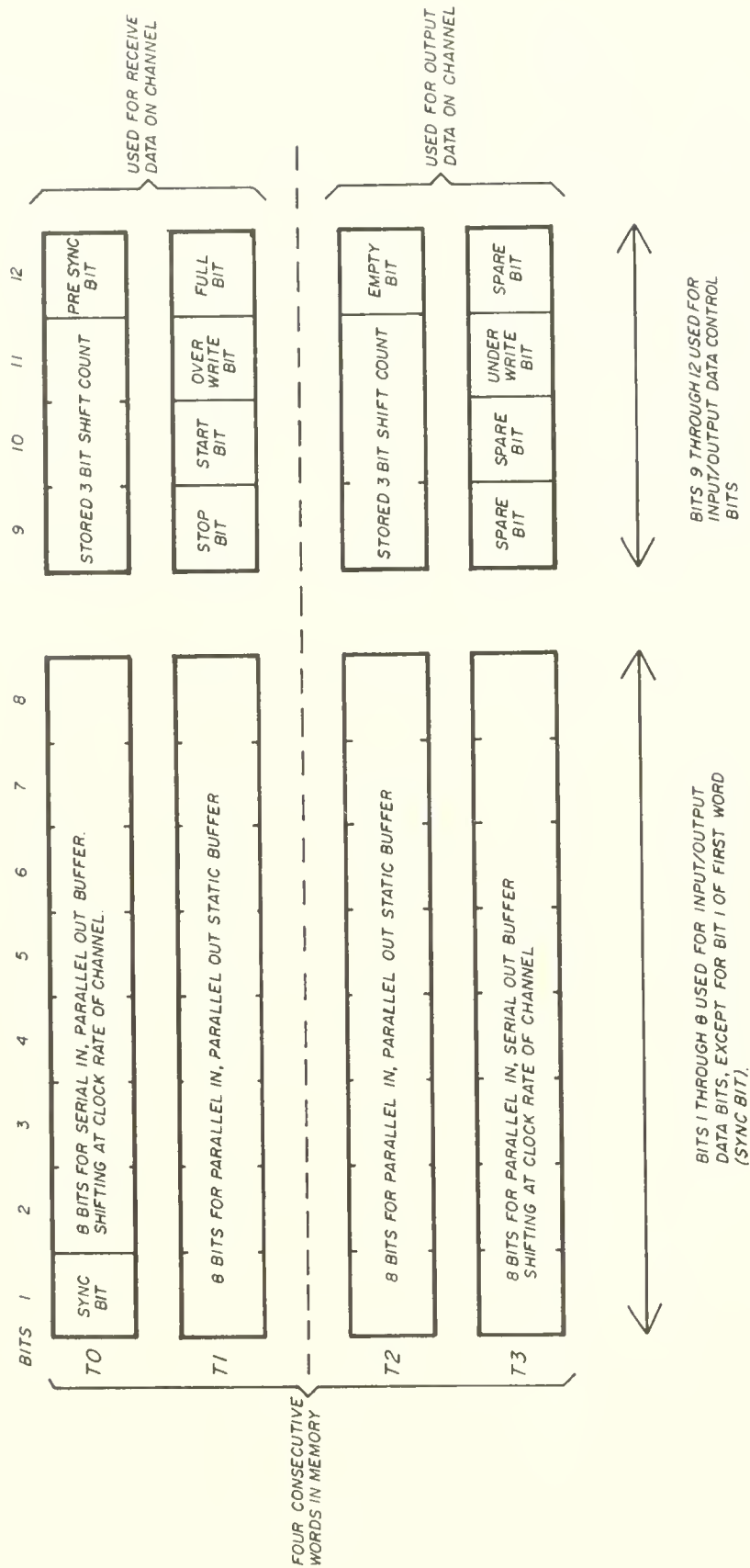
FIGURE 5 – BIT ASSIGNMENTS IN MEMORY FOR HANDLING ONE OF SIXTEEN SERIAL CHANNELS. TOTAL MEMORY REQUIREMENT IS 64 TWELVE BIT WORDS.

FIGURE 6 - DELAY LINE MEMORY

4 DELAY LINES USED FOR CONTROL BITS

DL 12

DL 11

DL 10

DL 9

1 MHZ CLOCK

ADD 1 LOGIC
(NAND GATES–NO DELAY)

8 DELAY LINES USED FOR DATA BITS

EXPANDABLE "OR" NODE

DL 8

DL 2

DL 1

1 BIT DATA DELAY

1 BIT DATA DELAY

1 BIT DATA DELAY

EIGHT 1 BIT DATA DELAY REGISTER
EACH IN SERIES WITH DATA DELAY LINE

SYNC COMPARE CIRCUITRY

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FIGURE 7 - MEMORY SYNCHRONIZATION

Labels within figure:

DELAY LINES

1 2 3 4 5 6 7 8   9 10 11 12

TO — 12 BIT MEMORY CELLS USED FOR RECEIVING
TI
T2 — 12 BIT MEMORY CELLS USED FOR TRANSMITTING
T3

4 µ SECONDS TIME SLICE FOR CHANNEL N

9 OF THE 64 12 BIT SEQUENTIALLY GENERATED WORDS IN MEMORY

TO
TI
T2
T3

4 µ SECONDS TIME SLICE FOR CHANNEL N+1

TO

DATA BITS   CONTROL BITS

MEMORY SYSTEM IS SYNCHRONIZED TO THE PRE-MULTIPLEXER
CHANNEL SCANNING SYSTEM. THEREFORE A GIVEN PRE-MULTIPLEXER
CHANNEL HAS ACCESS TO ONLY ONE GROUP OF FOUR 1µSEC WORDS
(TO,TI,T2,T3). 16 CHANNELS ARE HANDLED BY THIS SEQUENTIALLY
CONSTRUCTED MEMORY.

3D. Computer/Multiplexer Interface

(Appendix C Schematics, Sheets 18-28)

This section of the hardware contains two interfaces. They interface the delay line memory receive and transmit byte static buffers to the I/O bus of the computer. One interface contains the input data register, and the other the output data register. These registers provide the computer I/O bus with access to the delay line memory. A real time clock is used to pace the computer hardware interrupts for the 2 registers. The frequency of the clock depends upon the real time requirements of the channel with the highest bit rate.

Input Data Register System (Appendix C Schematics, Sheets 18, 19, 23)

When the byte storage buffers (word T1, Fig. 7) of the delay line memory become full, they compete for the input data register. When one byte is in this register, bytes are gated out until the register goes empty. The full condition of this register is gated with the pacing circuit. This generates an interrupt that causes the computer to enter an input routine.

When the input data register goes empty, it is ready to accept new bytes from the delay line memory. The process of the delay line memory emptying its byte storage buffers into the input data register continues until all receive byte buffers are empty.

As byte data is transferred from the delay line memory to the input data register, 4 bits from the clock, timing, and decode circuitry are strobed into 4 flip-flops of the register for channel identification. An additional 4 bits are strobed in the register. These are the overwrite, underwrite, start, and stop bits--see Fig. 5.

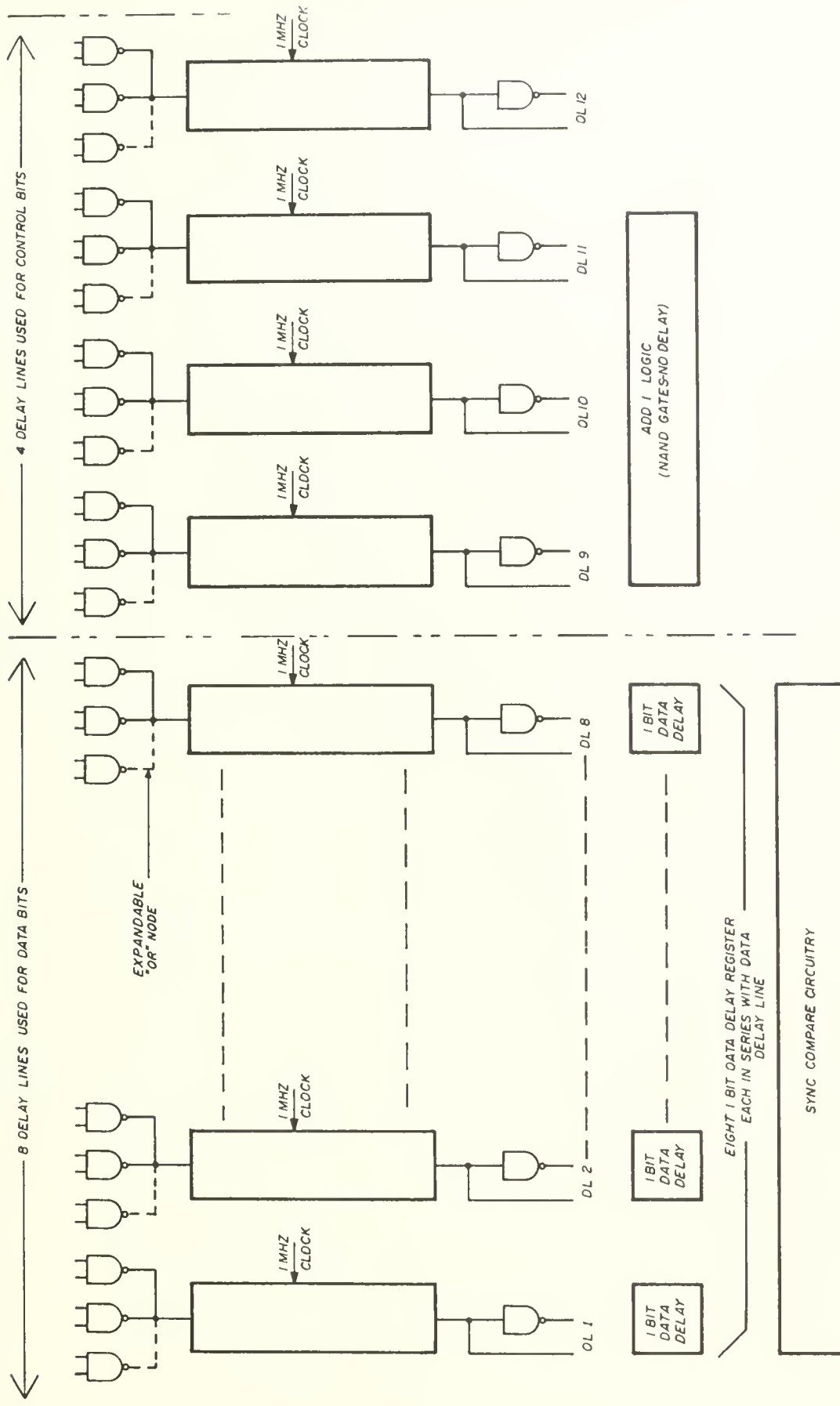The overwrite and underwrite bits are set only when the computer fails to satisfy the real time byte requirements of the channel for either the receive or transmit mode. The start bit is set to indicate to the computer the first byte of the receive message. The stop bit is set when the channel stops receiving.

Output Data Register (Appendix C Schematics, Sheets 20, 25-27)

When the byte static buffers (word T2, Fig. 7) of the delay line memory go empty, an empty-flag is set in the 16-bit delay line status register--Fig. 9. The empty-flag corresponds to the channel that went empty. The flag "or" output is gated with the pacing circuit for computer interrupt operation. The computer senses this empty-flag, and the empty/full status of the output data register-- Fig. 9. When the register is empty and the empty-flag is set, the computer is allowed to output a word for the corresponding transmitting channel. The computer output word is in the format shown in Fig. 9. The successful execution of this output resets the empty-flag in the 16-bit delay line status register. The empty-flag that gets reset is determined by the transmit channel 4-bit address, as indicated in the word format.

With the 16-bit delay line status register, the computer does not have to access the delay line memory (64 μsec access time) to check the empty/full status of a given byte static buffer. The register allows the computer to sense the condition without any memory (delay lines) access time. The importance of knowing this condition in advance is to prevent the computer from placing data, which the delay line memory will not accept, in the output data register.

The output data register, which stores byte data with its corresponding 4-bit channel address, remains full until the appropriate cell in the delay line memory is addressed by using the address compare circuit--Fig. 9. Since the total cycle time of the memory is 64 μseconds, the byte data transfer to memory will take place within this time. When the output data register goes empty, it is ready to accept new computer output data.

Interrupt Operation

There are two separate interrupts generated: one for all channels with receive byte data, and the other for all channels with transmit byte data. A real time clock is used to pace the interrupts.

The computer can then service the multiplexer in one routine for all transmitting channels, and one other routine for all receiving channels. This reduces the software overhead required for handling 16 serial data channels. The frequency of the interrupt

pacer must be selected to satisfy the byte level requirements of the serial channel with the highest bit rate.
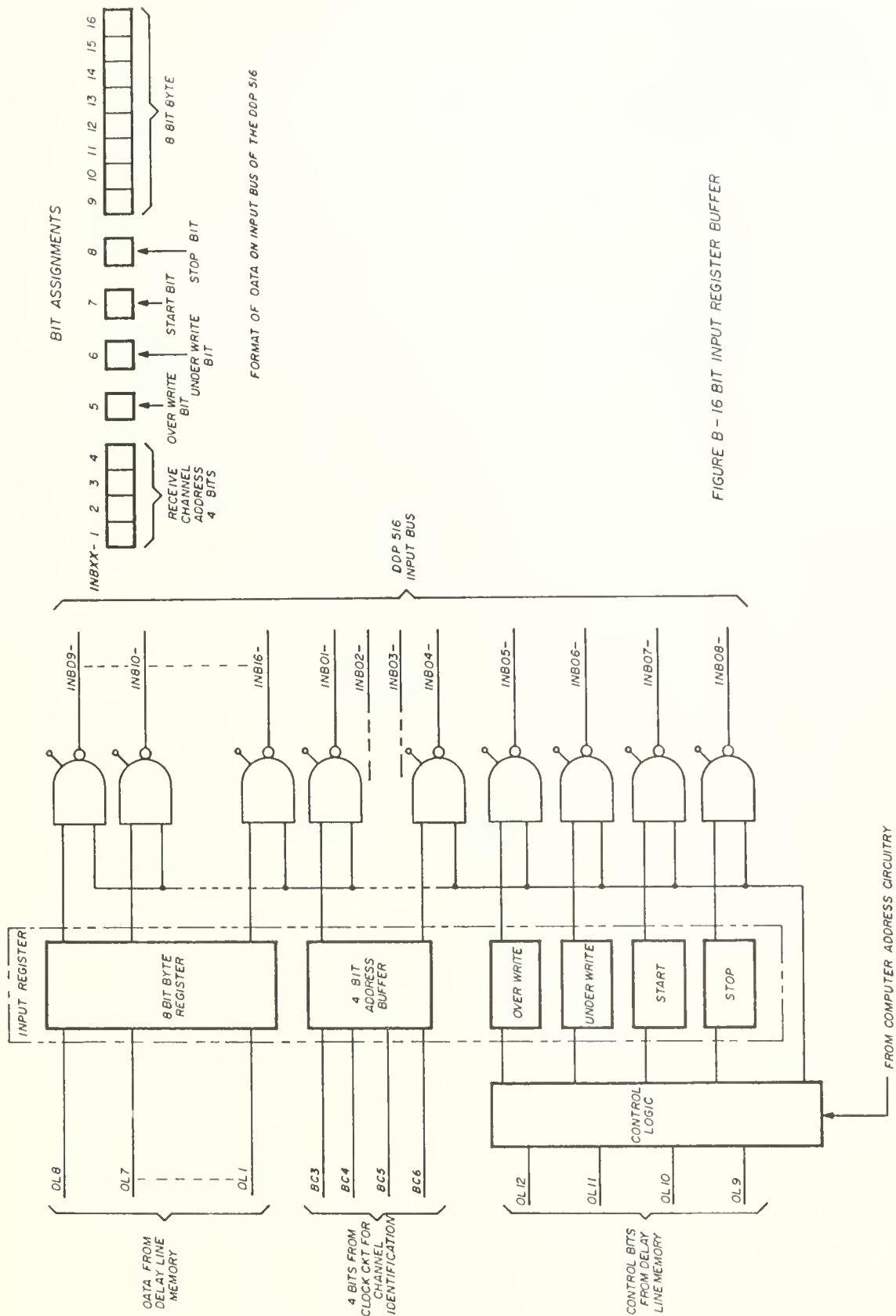
FIGURE B – 16 BIT INPUT REGISTER BUFFER

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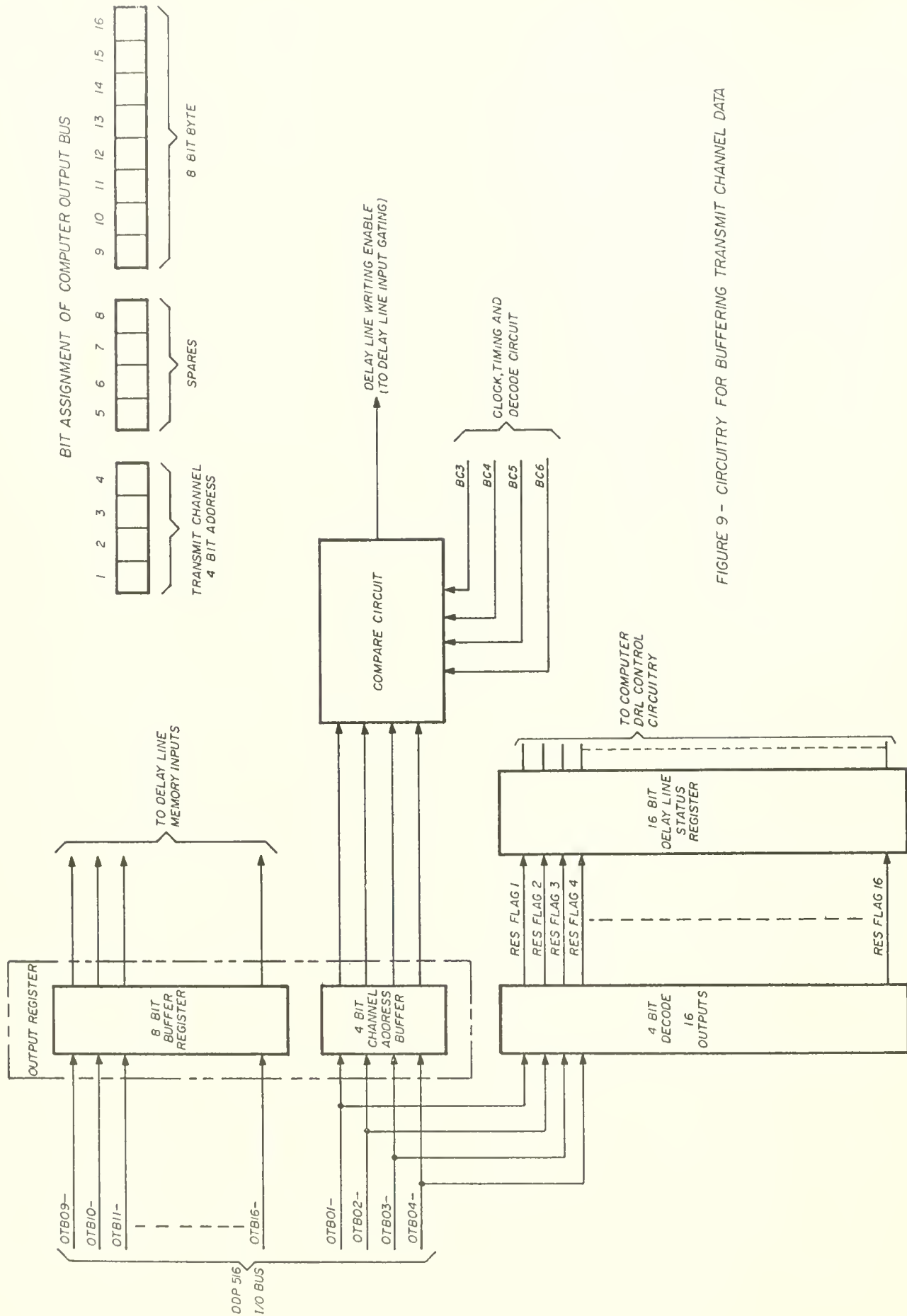
FIGURE 9 – CIRCUITRY FOR BUFFERING TRANSMIT CHANNEL DATA

4. SOFTWARE

4A. Software Specifications--Honeywell 16-Bit Series Machine

Interrupt Operation

SKS/430. Skip if not interrupting for input.

SKS/431. Skip if not interrupting for output.

SMK/020. Set mask for interrupting. A "1" in bit 3 of the A-register allows the multiplexer to interrupt for inputs. A "1" in bit 4 allows the multiplexer to interrupt for outputs. The master clear button on the computer console resets these bits.

Input Data to Computer

INA/1030. The program will skip the next instruction if the multiplexer is ready with data at the computer I/O bus. The next instruction is executed if the multiplexer is not ready to transfer data to the computer. The input data is in the format shown in Table III. Byte synchronization is performed in the multiplexer hardware. This feature can be bypassed on any individual channel if desired.

SKS/330. Skip if there are more inputs. If there are more inputs, the program may loop up to a maximum of 64 µseconds on the next INA/1030 instruction.

Outputing Data from the Computer to the Multiplexer

OTA/031. The program will skip the next instruction if the multiplexer accepts the output data. If it cannot accept the data,

the next instruction in the program is executed. The output data
is in the format shown in Table IV. When the OTA/031 instruction
is executed, the channel delay line byte buffer and the interface
register of the multiplexer must be empty in order for the output
data to be accepted.

SKS/331. Skip if there are any channel byte buffers empty.

SKS/231. Skip if the interface register is empty. The pro-
gram may loop to a maximum of 64 μseconds, since the multiplexer
hardware will empty the register within this time.

SKS/531. Specifying bits 1 through 4 of the output data for-
mat (Table IV) provides the test for the empty/full status of the
channel delay line byte buffer. This instruction is a skip if
empty.

Instructions for Setting Multiplexer Modes

OTA/131. This command unconditionally outputs a 16-bit word
to the multiplexer. Bits 1 through 16 of the A-register represent
channels 1 through 16. A "1" bit switches on the channel; a "0"
bit switches off the channel. The master clear button on the com-
puter console turns on all channels.

OTA/230. This command unconditionally outputs a 16-bit word
to the multiplexer. Bits 1 through 16 of the A-register represent
channels 1 through 16. A "1" bit sets the channel in the trans-
mit mode; a "0" sets the channel in the receive mode. The master
clear button on the computer console sets all channels to the
receive mode.

INA/1130. This command unconditionally inputs a 16-bit word from the multiplexer. Bits 1 through 16 represent channels 1 through 16. A "1" bit indicates that a valid user is connected to the channel. A "0" bit indicates that there is no valid user connected to the channel.

Table III -- Input Data Format

Bits	Function
1 through 4	4-bit address.
5	Overwrite bit. A "1" bit indicates that the computer is not satisfying the channel input real time requirements.
6	Underwrite bit. A "1" bit indicates that the computer is not satisfying the channel output real time requirements.
7	Start bit. A "1" bit indicates the first byte of the receive message.
8	Stop bit. A "1" bit indicates that the channel has stop receiving.
9 through 16	8 bit receive byte.

Table IV -- Output Data Format

Bits	Function
1 through 4	4-bit channel address
5 through 8	Spare bits
9 through 16	8-bit transmit byte

4B.   Computer I/O Examples

Multiplexer Input

The delay line memory is a sequential buffer which takes 64 μseconds to step through a complete cycle of memory. There is only one register between the delay line memory and the computer. If data can be accepted fast enough, the computer can do an effective scan of the delay line memory in 64 μseconds.

Straight line coding is an approach that can be used for an input scheme. In order that the computer completely scan the delay line memory for inputs, the three step input instruction set (DDP-516 computer) is repeated 22 times.

```
INPUT           BSZ   1
                INA   /1030
                JMP   *+2
                STA   BUFF 1
                ------------------
                INA   /1030
                JMP   *+2
                STA   BUFF 2
                ------------------
```

```
INA   /1030
JMP   *+2
STA   BUFF 3
- - - - - - - - - - - - - - - - - -
              .
              .
              .
              .
              .
INA   /1030
JMP   *+2
STA   BUFF 22
JMP   *  INPT
```

Multiplexer Output

When executing an OTA/031 instruction, the first 4 bits of
the computer A-register specify which of the 16 channels the out-
put data is for. In order for this instruction to be successfully
executed, the output register (computer/multiplexer interface) and
the byte static buffer (delay line memory) must be empty.

Again, as for inputing data to the computer, there is an
access problem. With the first 4 bits in the A-register, the
SKS/531 instruction can be used to check the status of the delay
line memory for a given transmit channel. Since the computer will
take 6.8 µseconds (DDP-516 computer) for each transmit channel out-
put, data should not be outputed for two adjacent channels consec-
utively. This is because a word can be written into the delay line
memory every 4 µseconds.

A program that can be used for outputing data to the multi-
plexer follows. It is continued until all channels that require
output data have been tried.

```
OUT             BSZ   1
                LDA   Chan 1
                SKS   /531
                JMP   *+4
                OTA   /031
                JMP   *-1
                JMP   *+2
                STA   SAV 1
        ----------------------------------
                LDA   Chan 3
                SKS   /531
                JMP   *+4
                ØTA   /031
                JMP   *-1
                JMP   *+2
                STA   SAV  3
        ----------------------------------
        Channel 5 data routine
        ----------------------------------
                        .
                        .
                        .
        ----------------------------------
        Channel 15 data routine
        ----------------------------------
        Channel 2 data routine
        ----------------------------------
                        .
                        .
```

.
.
.
.
.

Channel 16 data routine

'

5. APPENDICES

Appendix A. RS-232-B Serial Channel Standard

The RS-232-B standard serial data channel is terminated by a
25 pin Cinch connector. Signals on the input and output pins are
bi-polar DC levels: -6 volts or +6 volts. The connector pins
and their corresponding channel functions are as follows:

Pin 1--Protective Ground (AA)

Pin 2--Transmitted Data (BA). The terminal supplies the NRZ
   data stream to this pin. A logical "1" is -6 volts.
   A logical "0" is +6 volts.

Pin 3--Received Data (BB). This pin outputs the NRZ data
   stream to the terminal. A logical "1" is -6 volts.
   A logical "0" is +6 volts.

Pin 4--Request to Send (CA). When transmitting data onto the
   channel, the terminal equipment must supply +6 volts
   to this pin. When receiving data from the channel,
   the terminal equipment must supply -6 volts to this
   pin.

Pin 5--Clear to send (CB). This pin supplies a +6 volt trans-
   mit enable signal to the terminal. A -6 volt signal
   will inhibit the terminal from transmitting. When a

terminal issues a CA signal to the channel, the channel
will return, after a delay, a CB signal to the terminal.

Pin 6--Data Set Ready (CC). This pin supplies a +6 volt sig-
nal to the terminal to indicate when the channel can
transmit or receive data. Ground indicates that the
channel is not ready for communicating.

Pin 7--Signal Ground (AB).

Pin 8--Data Carrier Detector (CF). This pin supplies +6 volts
to the terminal to indicate the presence of the Receive
Clock (DD). -6 volts indicates the absence of DD.

Pin 9--Reserved for data set testing.

Pin 10-Reserved for data set testing.

Pin 11-Unassigned.

Pin 12-Unassigned.

Pin 13-Unassigned.

Pin 14-Unassigned.

Pin 15-Channel Transmit Clock (DB). This pin supplies a ±6
volt square wave to the terminal equipment when trans-
mitting data into the channel. The positive transition
of DB is used for shifting data on to the BA line from
the terminal.

Pin 16-Unassigned.

Pin 17-Receiver Clock (DD). This pin supplies a ±6 volt square
wave to the terminal equipment when receiving data from
the channel. The BB line presents a new data bit at the

positive transition of DD.

Pin 18-Unassigned.

Pin 19-Unassigned.

Pin 20-Data Terminal Ready (CD). The terminal supplies +6
volts to this pin to indicate it is ready to operate.
-6 volts indicates a not ready condition.

Pin 21-Unassigned.

Pin 22-Ring Indicator (CE). This pin supplies the terminal
with +6 volts to indicate that there is a remote user
trying to establish a communications link through the
channel. Otherwise this pin is at -6 volts.

Pin 23-Unassigned.

Pin 24-External Transmit Clock (DA). The terminal supplies
to this pin a ±6 volt square wave when the transmitted
data through the channel is to be clocked by the ter-
minal equipment.

Pin 25-Unassigned.

Appendix B. Honeywell 16-Bit Series Standard I/O Channel

The Honeywell 16-bit series standard I/O channel is a shared
bus I/O system that consists basically of 48 twisted lead pairs.
Thirty pairs are used for output and 18 pairs for input.

The 30 output twisted lead pairs are:

16-for data bits (OTBXX)

10-for address bits (ADBXX)

1-for reset ready (RRL)

1-for output command (OCP)

1-for master clear (MSTCL)

1-for set mask (SMSK)

The 18 input twisted lead pairs are:

16-for data bits (INBXX)

1-for device ready (DRL)

1-for program interrupt (PIL)

Signals on the output and input leads are DC levels: 0 or
-6 volts in the DDP-116 and 0 or +6 volts in the DDP-416, DDP-516,
and H-316. All leads are shared with all interfaces. Memory access
I/O channels are available as options for all these 16-bit computers

The channel is synchronized by a specific time sequence of events. For example, within the I/O instructions there exist the following sequence of events: (a) an address goes out on the address bus, (b) a device decodes this address and responds, and (c) a strobe for the device terminates the instruction. The standard channel provides a hardware program interrupt feature to service devices on demand. The standard channel is a parallel I/O bus that is shared by all interfaces under program control.

The I/O software instructions and their hardware significance are discussed briefly.

Output Command (OCP)

This instruction initiates DC levels on the 10-bit address bus and a delay pulse on the output command twisted pair. This instruction is used to control the functioning of the I/O device, and expects no response from the device.

Sense Condition (SKS)

This instruction initiates DC levels on the 10-bit address bus and senses the input device ready lead. When a signal appears on this lead, during a set time in the instruction period, it causes the next instruction to be skipped. If no signal appears, the next instruction will be executed. This (SKS) instruction is used to test conditions of specific interfaces on the I/O bus.

Single Word Input (INA)

The input instruction initiates action by placing DC levels on the 10-bit address bus. The addressed interface then places its input data on the 16-bit input bus; simultaneously, a signal is placed on the input device ready lead. The computer will acknowledge the input with a signal on the output reset ready lead, and will skip the next instruction to be executed. In the event of no input, the addressed interface does not return a device ready signal. The computer does not skip the next instruction, nor acknowledge an input with a signal on the reset ready lead. Multiple word inputs must be accomplished by creating a program loop of single word (INA) inputs.

Single Word Output (ØTA)

The output instruction initiates action by placing DC levels on the 10-bit address bus and the 16-bit output bus. The addressed interface accepts the data by placing a signal on the input device ready lead. The computer will then respond on the reset ready lead with a signal which can be used as a strobe for the output data. The computer will then skip the next instruction to be executed. In the event the addressed interface does not accept the output, the computer will not skip the next instruction, nor respond with a signal on the reset ready lead. Multiple word outputs must be accomplished by creating a program loop of single word (ØTA) outputs.

Any interface on the I/O bus can initiate an interrupt by placing a DC level on the program interrupt lead (PIL). Since this lead is common to all interfaces, when an interrupt occurs a program using the sense condition instruction (SKS) must be used to seek out the source of interrupt, and then jump to a subroutine to service it. Priorities of program interrupts are accomplished through the use of mask bits. Each interface is assigned a bit which is used to generate its program interrupt (PIL) signal.

Refer to Honeywell Interface Manual (Pub. No. 130071624) for further details on the I/O channel of the 16-bit series computers.

Appendix C. System Schematics
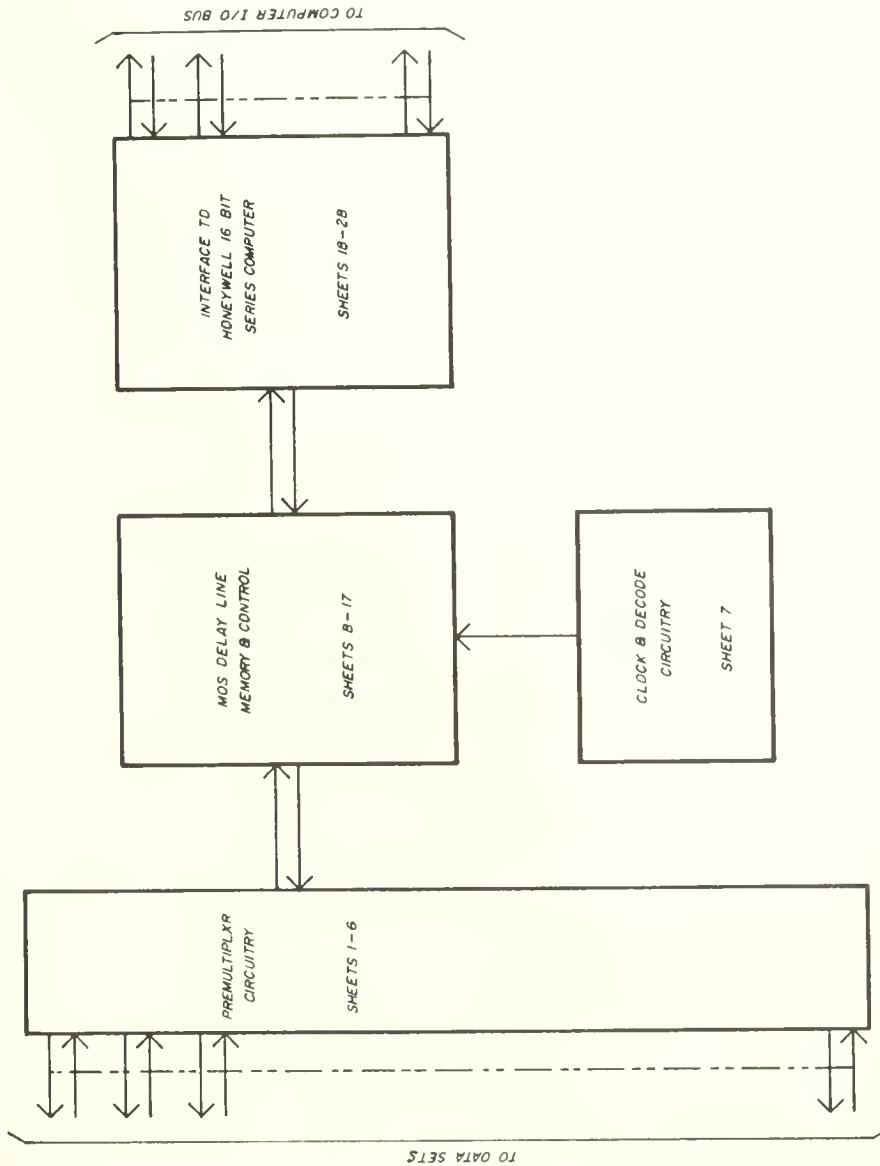
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TITLE 16 PORT DATA SET MULTIPLXR

REV DATE
10-13-70

TO COMPUTER I/O BUS

INTERFACE TO
HONEYWELL 16 BIT
SERIES COMPUTER

SHEETS 18-28

MOS DELAY LINE
MEMORY B CONTROL

SHEETS 8-17

CLOCK B DECODE
CIRCUITRY

SHEET 7

PREMULTIPLXR
CIRCUITRY

SHEETS 1-6

TO DATA SETS

47

49

TABLE THREE

CKT	(ac)	(ab)	(bb)	(*)
3	A28	C17	01	2
7	A26	A12	06	3
11	A24	C67	12	4
15	A22	A62	16	5

TO LEVEL CONVERTOR BLOCK
CONNECT μ-PAC CABLE 'A'(SHT 5)
TO POSITION (bb), SEE TABLE THREE

NOTE: ALL EQUIPMENT ON THIS SHEET
IS ON RACK NO 2

RS(XX) 7
C(*)2
RS(XX) 7
LC"Y" 28
C(*)4
C(*)4
LC"Y" 2
DTR(XX) 8

RO(XX) 3
CR(XX) 3

DSR(XX) 6
3D1
RC(XX) 2

TC(XX) 4
CTS(XX) 5

-11 32
DD 401
LC"Y" 10
TO(XX) 9
-6V

CONNECT μ-PAC CABLE TO POSITION(ac),(SEE TABLE THREE) B SHT 6,F0
TO HUB, RACK NO 1
(CONNECT μ PAC CABLE TO POSITION(bb), (SEE TABLE THREE) B SHT 6,F0

C(*)8 — SEE TABLE THREE
OTB(XX)

SET DTR
SET RS
MC₁

ORI-
ORRM-
DSR(XX) 306

RRFS-
CTS·RS(XX)

TRFS-

ORTM-
SEE TABLE THREE

TD COM (A)-
TD COM

RORI₁
TD GATE

53

TABLE FIVE

DATA SET	(xx)	(xy)	(aa)	(bb)	(cc)	(dd)	(ee)	(ff)	(gg)	(hh)	(jj)
1	01	1	C27	A17	A16	A15	–	–	A18	2	1
2	02	2	C27	A17	A16	–	B18	B17	A18	2	–
3	03	3	C22	C17	C16	C15	–	–	C18	4	3
4	04	4	C22	C17	C16	C14	B16	B15	C18	4	–
5	05	1	C37	C12	C13	C14	–	–	C11	6	5
6	06	2	C37	C12	C13	–	–	B14	C11	6	–
7	07	3	C32	A12	A13	–	B13	B14	A11	8	7
8	08	4	C32	A12	A13	A14	B11	B12	A11	8	–
9	09	1	C47	A67	A66	A65	–	–	A69	10	9
10	10	2	C47	A67	A66	–	868	867	A68	10	–
11	11	3	C42	C67	C66	C65	–	–	C68	12	11
12	12	4	C42	C67	C66	C64	868	B65	C68	12	–
13	13	1	C57	C62	C63	–	–	B63	C61	14	13
14	14	2	C57	C62	C63	464	864	B64	C61	14	–
15	15	3	C52	A62	A63	464	B61	B62	A61	16	15
16	16	4	C52	A62	–	–	B61	–	A61	16	–

TO PRE-MULTIPLEXOR

90 CABLE B₁

TO ODD NUMBER DATA SET (jj)

CABLE B₂

TO EVEN NUMBER DATA SET (hh)

TO DATA SETS

10 CONDUCTOR CABLES

CONNECTOR NO 1 (TO ODD NO DATA SETS)
CONNECTOR NO 2 (TO EVEN NO. DATA SETS)

CINCH PAT 2790153
DB19604.432 MALE CONN
25 PIN

TERM NO. U-PAC	SIGNAL		DATA SET CONN
2	RD--		3
3	RC--		17
4	CR--		8
5	TC--		15
6	CTS--	CONN	5
7	DSR--	NO 1	6
8	RS--		4
9	DTR--		20
32	TD--		2
	GRD		7 (STRAP 7 B 1)
11	RD--		3
12	RC--		17
13	CR--		8
14	TC--		15
15	CTS--	CONN	5
16	DSR--	NO 2	6
17	RS--		4
18	DTR--		20
19	TD--		2
33	GRD		7 (STRAP 7 B 1)

TO ODD NO DATA SETS

TO EVEN NO DATA SETS

CABLE B₁

RD(xx) RC(xx) CR(xx) TC(xx) CTS(xx) DSR(xx) RS(xx) DTR(xx) TD(xx) GRD

CABLE B₂

RD(xx) RC(xx) CR(xx) TC(xx) CTS(xx) DSR(xx) RS(xx) DTR(xx) TD(xx) GRD

(gg)

(cc) (dd) (ee) (ff)

LC "X" (a) 23 / 28
LC "X" (b) 11 / 21
LC "X" (c) 4 / 9

SEE TABLE 5

(bb)

CABLE A

(aa)

RD(xx) RC(xx) CR(xx) TC(xx) CTS(xx) DSR(xx) RS(xx) DTR(xx) TD(xx) GRD

RD(xx) RC(xx) CR(xx) TC(xx) CTS(xx) DSR(xx) RS(xx) DTR(xx) TD(xx) GRD

PREMULTIPLEXOR SEE SHEET (XY)

ODD CIRCUITS

EVEN CIRCUITS

TABLE 6

A'6 PRE-MULT LOCATION	B'6 SIGNAL	C'6 PIN NO	D'6 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4DO	DSR16	28	23F4
3DO	DSR15	27	23E4
2DO	DSR14	26	23E4
1DO	DSR13	25	23D4
4FO	17	24	7C9
3FO	16	23	7C9
2FO	15	22	7C9
1F7	14	21	7B9
1DO	13	20	7B9
4DO	CTSRS16	19	26G4
3DO	CTSRS15	18	26E4
2DO	CTSRS14	17	26D4
1DO	CTSRS13	16	26B4
4AO	OTB16	15	27DO
3AO	OTB15	14	27DI
2AO	OTB14	13	27DI
1AO	OTB13	12	27D2
1EO	ROR II,	11	8D9
1GO	TD GATE	10	8C9
1FO	TD COM-	9	8F9
1FO	ORTM-	8	8BO
1EO	TRFS-	7	8FO
1CO	ORRM-	6	8AO
1CO	RRFS-	5	8EO
1CO	ORI-	4	8GO
1BO	MC,-	3	22DO
1BO	SET RS	2	21C9
1BO	SET DTR	1	21B9

TABLE 7

A'7 PRE-MULT LOCATION	B'7 SIGNAL	C'7 PIN NO	D'7 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4DO	DSR12	28	23C4
3DO	DSR11	27	23C4
2DO	DSR10	26	23B4
1DO	DSR09	25	23B4
4FO	13	24	7B9
3FO	12	23	7B9
2FO	11	22	7A9
1F7	10	21	7A9
1DO	07	20	7F9
4DO	CTSRS12	19	26GO
3DO	CTSRS11	18	26EO
2DO	CTSRS10	17	26DO
1DO	CTSRS09	16	26BO
4AO	OTB12	15	2703
3AO	OTB11	14	2703
2AO	OTB10	13	27D4
1AO	OTB09	12	27D4
1EO	ROR II,	11	8D9
1GO	TD GATE	10	8C9
1FO	TD COM-	9	8F9
1FO	ORTM-	8	8BO
1EO	TRFS-	7	8FO
1CO	ORRM-	6	8AO
1CO	RRFS-	5	8EO
1CO	ORI-	4	8GO '
1BO	MC,-	3	22DO
1BO	SET RS	2	21C9
1BO	SET DTR	1	21B9

TABLE 8

A'8 PRE-MULT LOCATION	B'8 SIGNAL	C'8 PIN NO	D'8 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4DO	DSR 08	28	23FI
3DO	DSR 07	27	23EI
2DO	DSR 06	26	23DI
1DO	DSR 05	25	23DI
4FO	07	24	7F9
3FO	06	23	7F9
2FO	05	22	7E9
1F7	04	21	7E9
1DO	03	20	7E9
4DO	CTSRS 08	19	25G4
3DO	CTSRS 07	18	25E4
2DO	CTSRS 06	17	25D4
1DO	CTSRS 05	16	25B4
4AO	OTB08	15	27D5
3AO	OTB07	14	27D5
2AO	OTB06	13	27D6
1AO	OTB05	12	27D7
1EO	ROR II,	11	8D9
1GO	TD GATE	10	8C9
1FO	TD COM-	9	8F9
1FO	ORTM-	8	8BO
1EO	TRFS-	7	8FO
1CO	ORRM-	6	8AO
1CO	RRFS-	5	8EO
1CO	ORI-	4	8GO
1BO	MC,-	3	22DO
1BO	SET RS	2	21C9
1BO	SET DTR	1	21B9

TABLE 9

A'9 PRE-MULT LOCATION	B'9 SIGNAL	C'9 PIN NO	D'9 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4DO	DSR 04	28	23CI
3DO	DSR03	27	23CI
2DO	DSR 02	26	23BI
1DO	DSROI	25	23BI
4FO	03	24	7E9
3FO	02	23	7E9
2FO	01	22	709
1FO	00	21	709
1DO	17	20	7C9
4DO	CTSRS 04	19	25EO
3DO	CTSRS 03	18	25EO
2DO	CTSRS 02	17	2500
1DO	CTSRS 01	16	2580
4AO	OTB04	15	2707
3AO	OTB03	14	27D8
2AO	OTB02	13	27D8
1AO	OTBOI	12	27D9
1EO	ROR II,	11	8D9
1GO	TD GATE	10	8C9
1FO	TD COM-	9	8F9
1FO	ORTM-	8	8BO
1EO	TRFS-	7	8FO
1CO	ORRM-	6	8AO
1CO	RRFS-	5	8EO
1CO	ORI-	4	8GO
1BO	MC,-	3	22DO
1BO	SET RS	2	21C9
1BO	SET DTR	1	21B9

HUB (RACK 1)

- A22 (C'6) (B6) — (D6) — SEE TABLE 6
- A24 (C'7) (B7) — (D7) — SEE TABLE 7
- A26 (C'8) (B8) — (D8) — SEE TABLE 8
- A28 (C'9) (B9) — (D9) — SEE TABLE 9

CABLE A3 (DATA SETS 13-16)
CABLE B3 (DATA SETS 9-12)
CABLE C3 (DATA SETS 5-8)
CABLE D3 (DATA SETS 1-4)

PRE-MULT (RACK 2)

- C58 (C'6) (B6) (A6) — SEE TABLE 6
- C48 (C'7) (B7) (A7) — SEE TABLE 7
- C38 (C'8) (B8) (A8) — SEE TABLE 8
- C28 (C'9) (B9) (A9) — SEE TABLE 9

CLOCK B DECODE CIRCUIT

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ENG. V P   DR. BY A.M.K.   DATE 7-/0-70
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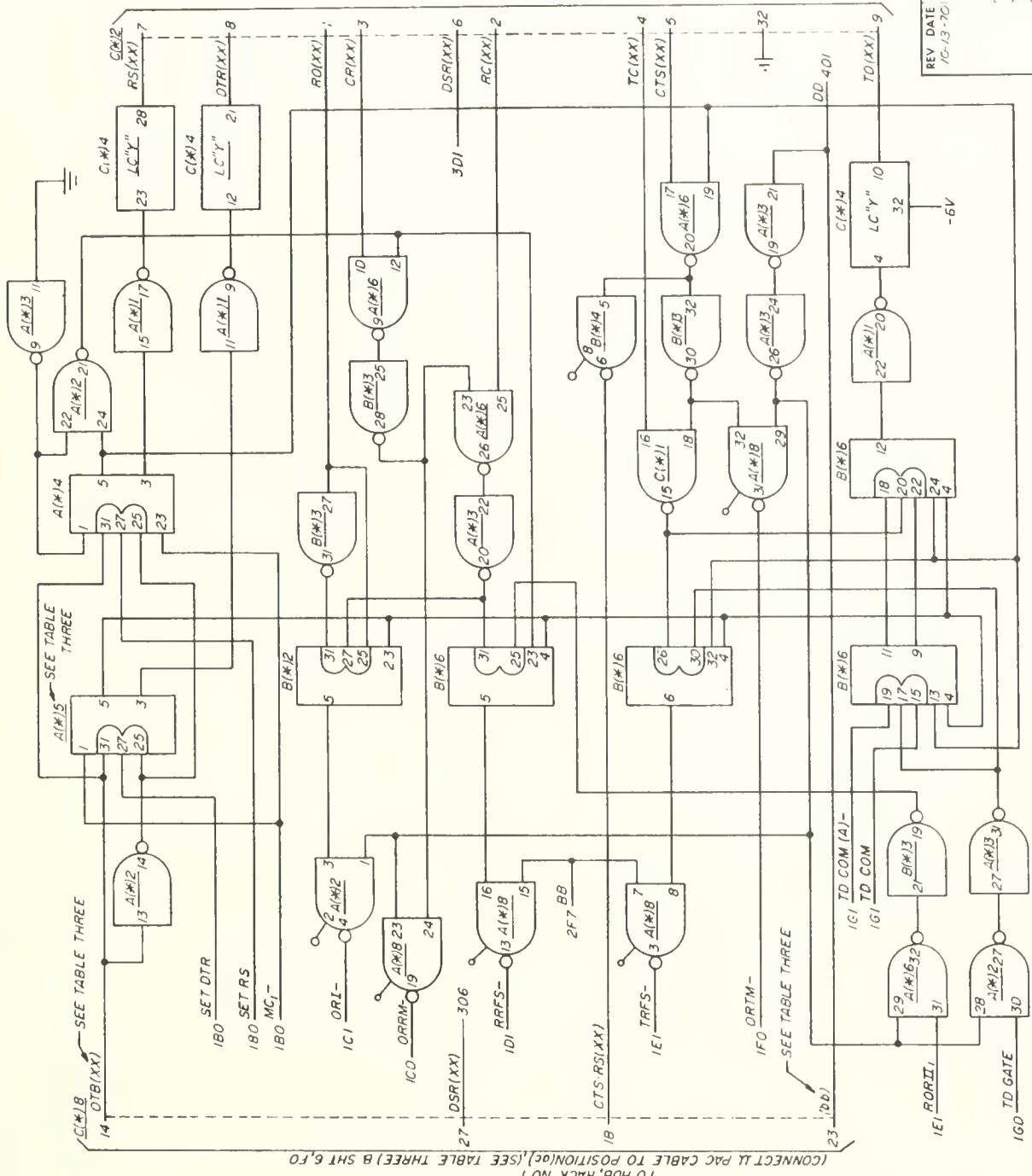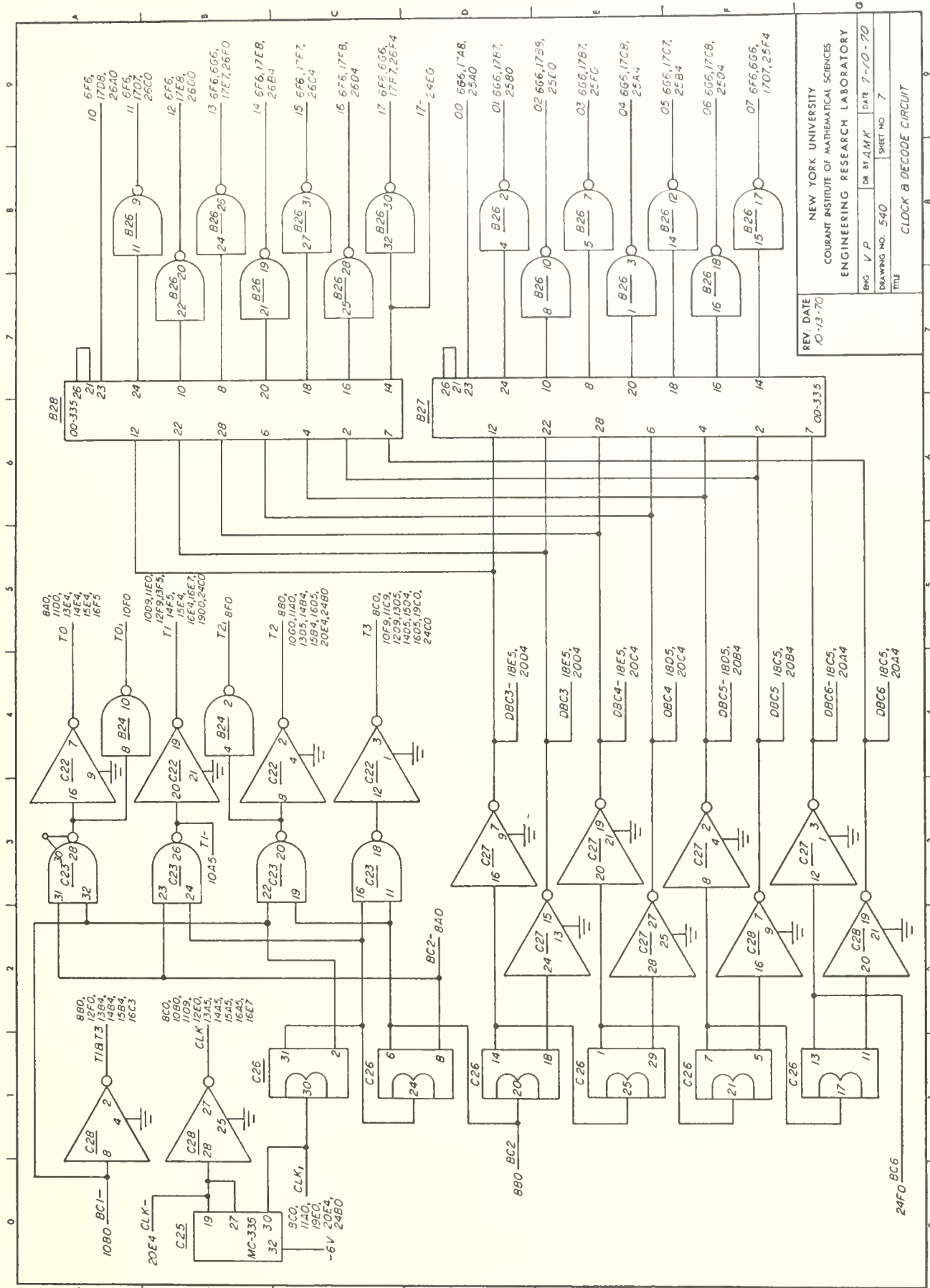NEW YORK UNIVERSITY
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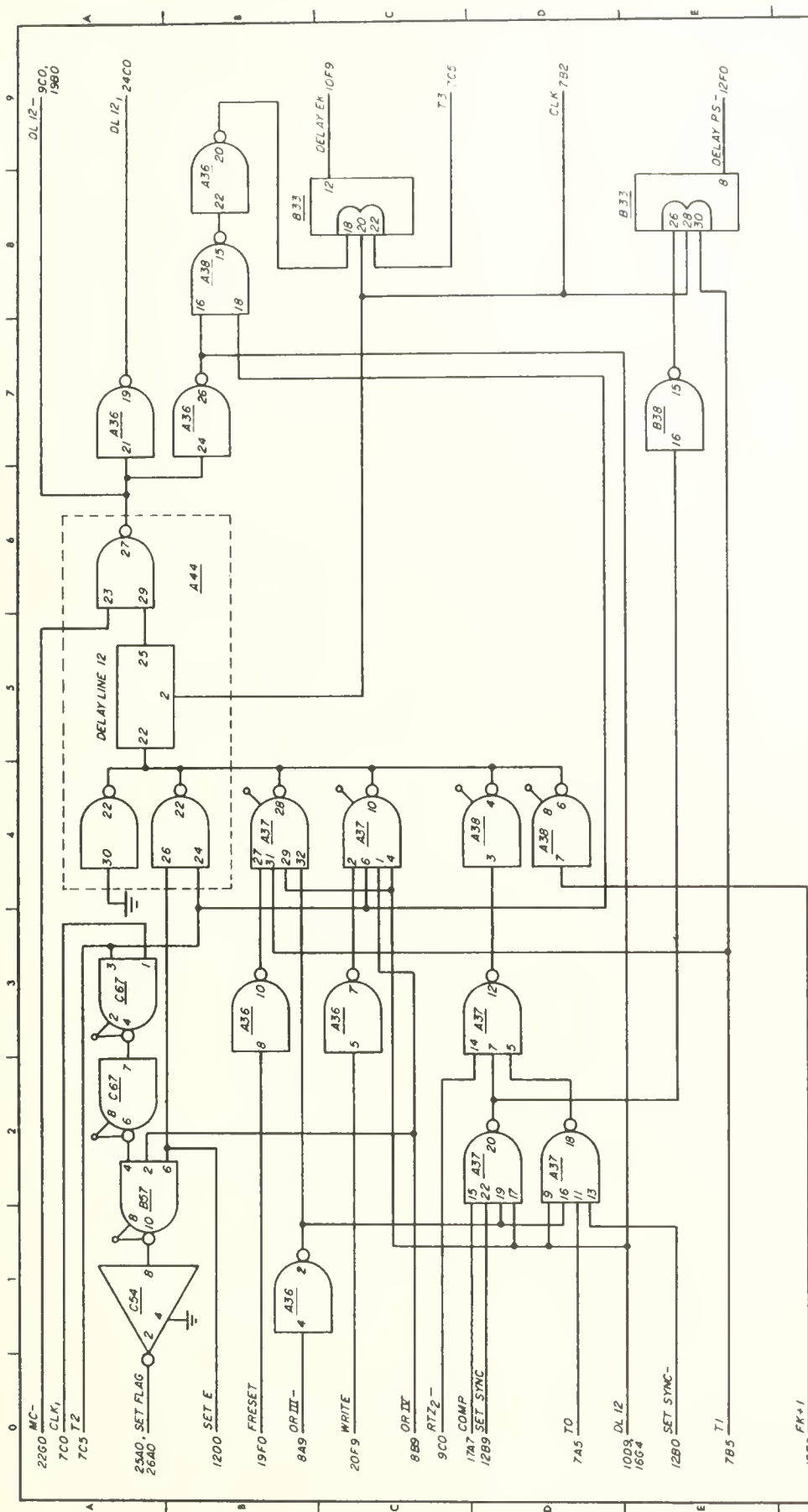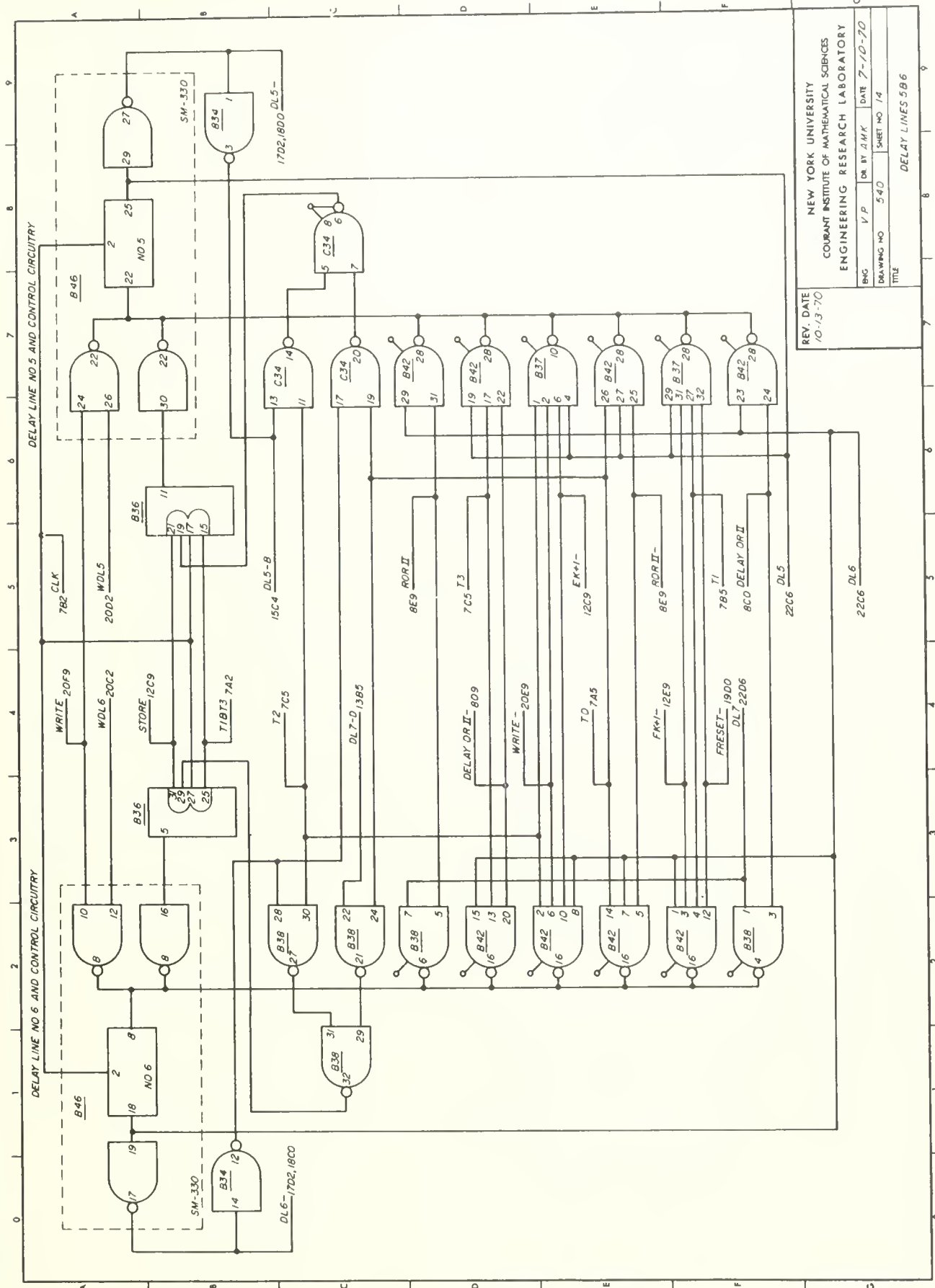| DRG | V.P | DR BY | J.M.K | DATE | 7-10-70 |
| DRAWING NO | 540 | SHEET NO | 8 | | |

TITLE PREMULTIPLXR TO HUB SYNCHRONIZER

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TITLE	DELAY LINE 9,10B11

REV DATE
10-13-70

DL-2 11DC
OR III- 849
DI-D 9C0
FK+1 11F0,12E9
T1 7B5
OVRESET- 1900
DELAY EK+1- 1209
UWRESET- 19E0
T3 7C5
OR IV 889
DELAY EK 11C9
DELAY EK+1 1209

T1- 7B3
AK- 9A0,19E0
AK 22E6
BK 22E6
BK- 9B0,19B0
CK 22F6
CK- 9B0

DELAY LINE 9
DELAY LINE 10
DELAY LINE 11
A46
A46
A44
A47
A47

849 OR III
7B2 CLK
19F0 PRESET
949 AK+1
7A0 BC1-
909 BK+1
745 T0,
9E9 CK+1
7C5 T2

B34
B34
B34
B37
B35
B38
A42
A42
A42
A42
B24

SET SYNC 11D0,16G4

EK+1- 13E5,14E5, 15E5,16E5

STORE 13A4,14B4, 15B4,16A3

T3 7C5

DELAY EK+1- 10E9

DELAY EK+1 10F9

DELAY SK 16D9

FK+1 10D9,11F0

FK+1- 13E4,14E4, 15F5,16E5

STRIP SYNC- 17A7

T1 7B5

11 E0 SET SYNC-

8E9 RCC +I

6E9 EK+1-

9E9 EK+1-

11B0 SET E

9F9 CK+1-

8F9 STORE +I

7B2 CLR

7A2 T1 6 +3

11E9 DELAY PS-

DELAY LINE NO. 7 AND CONTROL CIRCUITRY
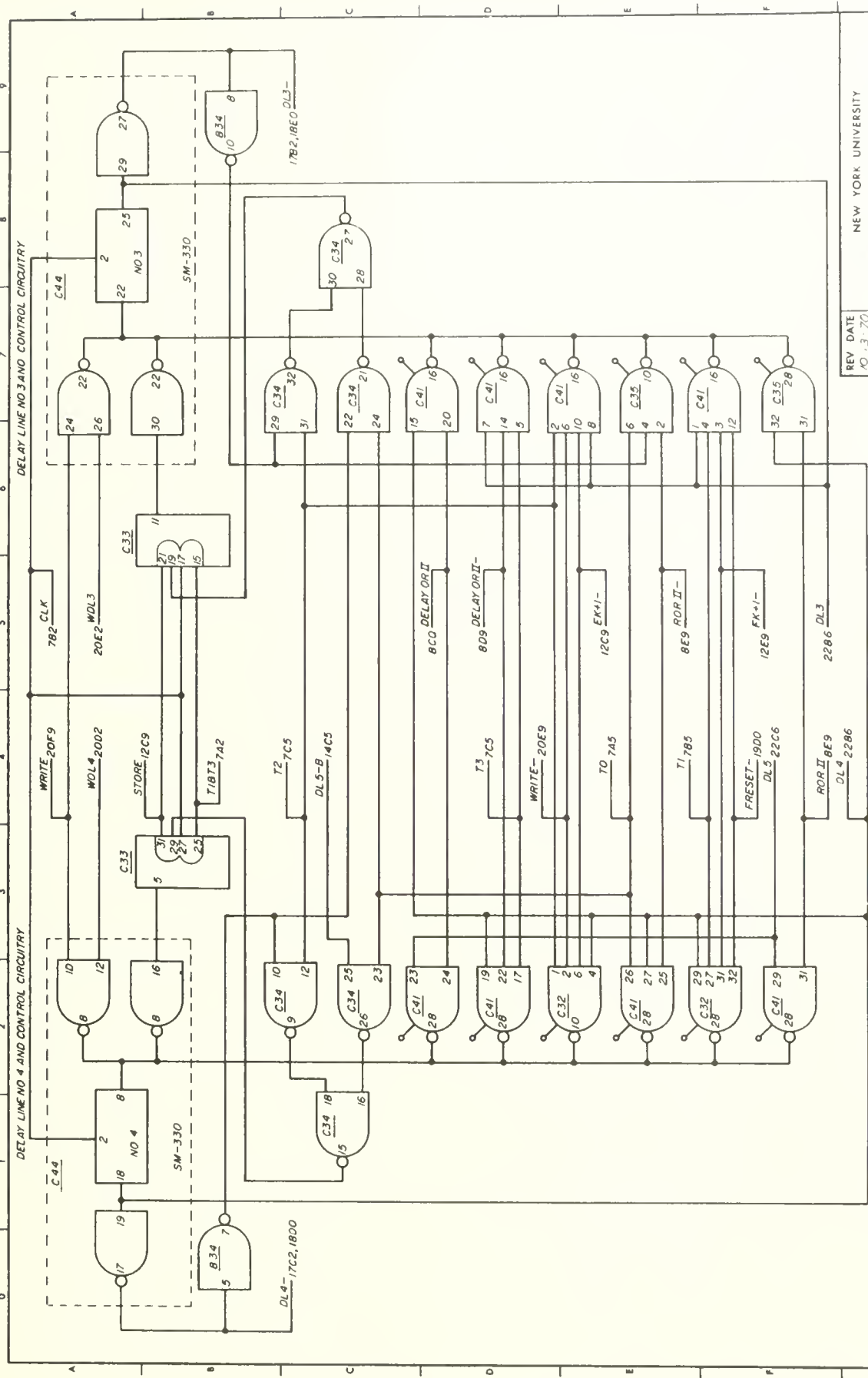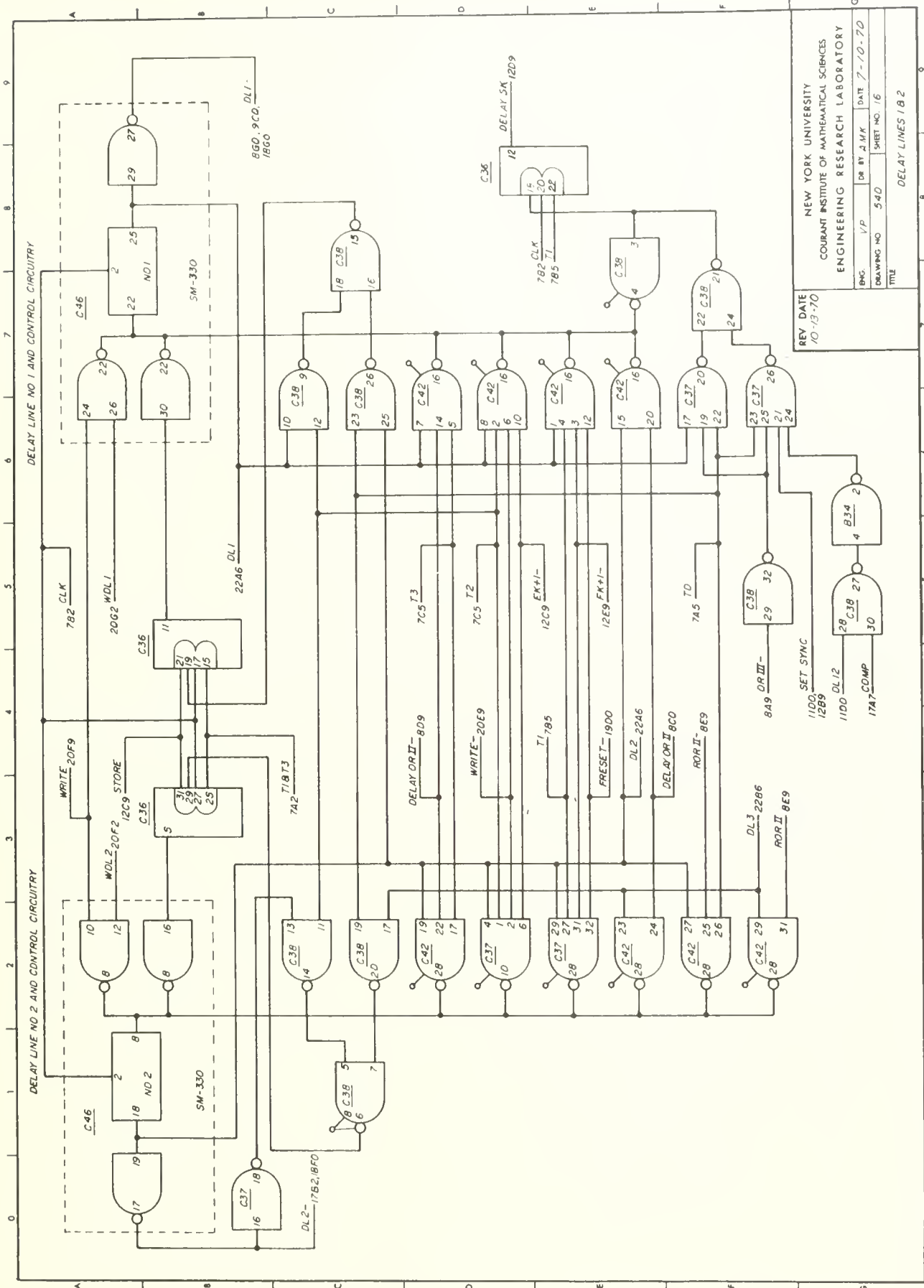
DELAY LINE NO.8 & CONTROL CIRCUITRY

REV DATE
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ENG	V.P.	DR BY A.MK	DATE 7-10-70
DRAWING NO 540		SHEET NO. 13	
TITLE			

DELAY LINES 788

73

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DELAY LINES 5&6

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ENG.	V.P.	DR BY	2 MK	DATE	7-10-70
DRAWING NO	540	SHEET NO	16
TITLE	DELAY LINES 1 & 2

REV DATE
10-13-70

STRIP SYNC CABLE PAC

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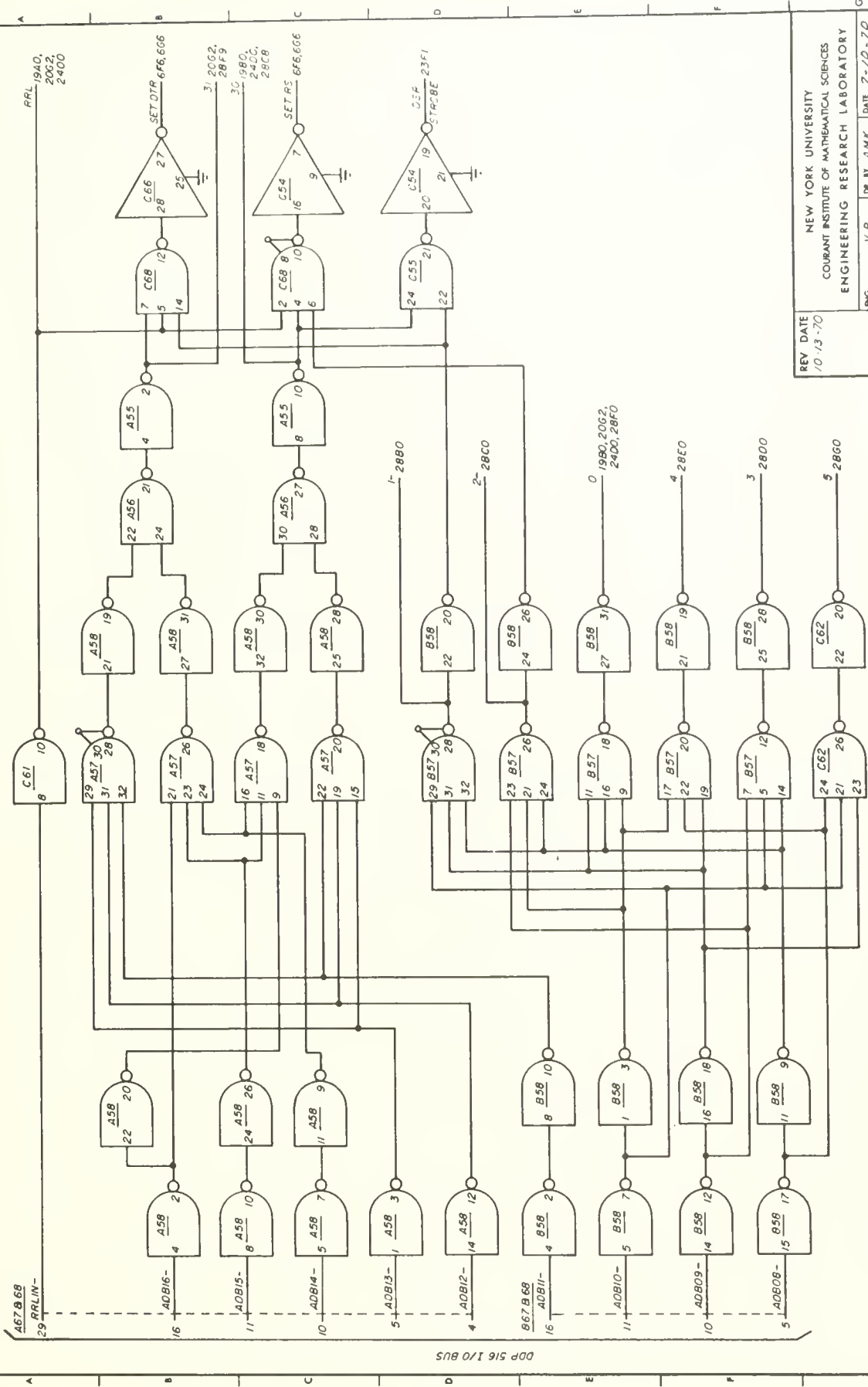| ENG | VP | DR BY AMK | DATE 7-10-70 |
| DRAWING NO | 540 | SHEET NO. 17 | |
| TITLE | COMPARE B STRIP SYNC CIRCUIT | | |

REV. DATE
10-13-70

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ENG	V P	DR BY A MK	DATE 7-10-70
DRAWING NO	540	SHEET NO 18	
TITLE	DDP 516 INPUT BUFFER		

REV. DATE
10-13-70

89

OL1 16B5
OL2 16E4,17A1
OL3 15F5,16F3, 17B1
OL4 15G4,17C1
OL5 14F5,15F4, 17C1
OL6 14G5,17D1
OL7 13F5,14F4, 17E1
OL8 13F4,17E1
AK 9A0,10C5
BK 9B0,10D5, 19G0
CK 9B0,10F5, 19D0
MC5 - 18A8
MC4 20G0
MC3 8D0,18F8, 20D2

C52 2 / 6
C52 10 / 6
C52 7 / 6
C52 3 / 6
C52 12 / 13
C52 18 / 13
C52 17 / 13
C52 9 / 13
C52 28 / 25
C52 30 / 32
B55 4 / 1
C51 31 / 29
C51 28 / 29
C51 30 / 29

C51 20 / 22
C51 26 / 24

INP MSK 28A0
OUT MSK 28B0

B61 12 / 18 20 22 24
B61 6 / 26 28 30 32

C66 15 / 24 13
C66 3 / 12 14 1

C61 2 / 4
B63 30 / 32

MC1 -
6F6,6G6 -

A67B68
MSTCL - 31
PWRFL - 23
B67B68
SMKO1 - 29
MC
24F0,25B0,
26B0

DOP 516 I/O BUS

OTB03
2708

OTB03 -
2708

OTB04
2707 OTB04
2707 OTB04 -
MC -
11A0,19A8,
20F2

91

DSR INPUT BUS

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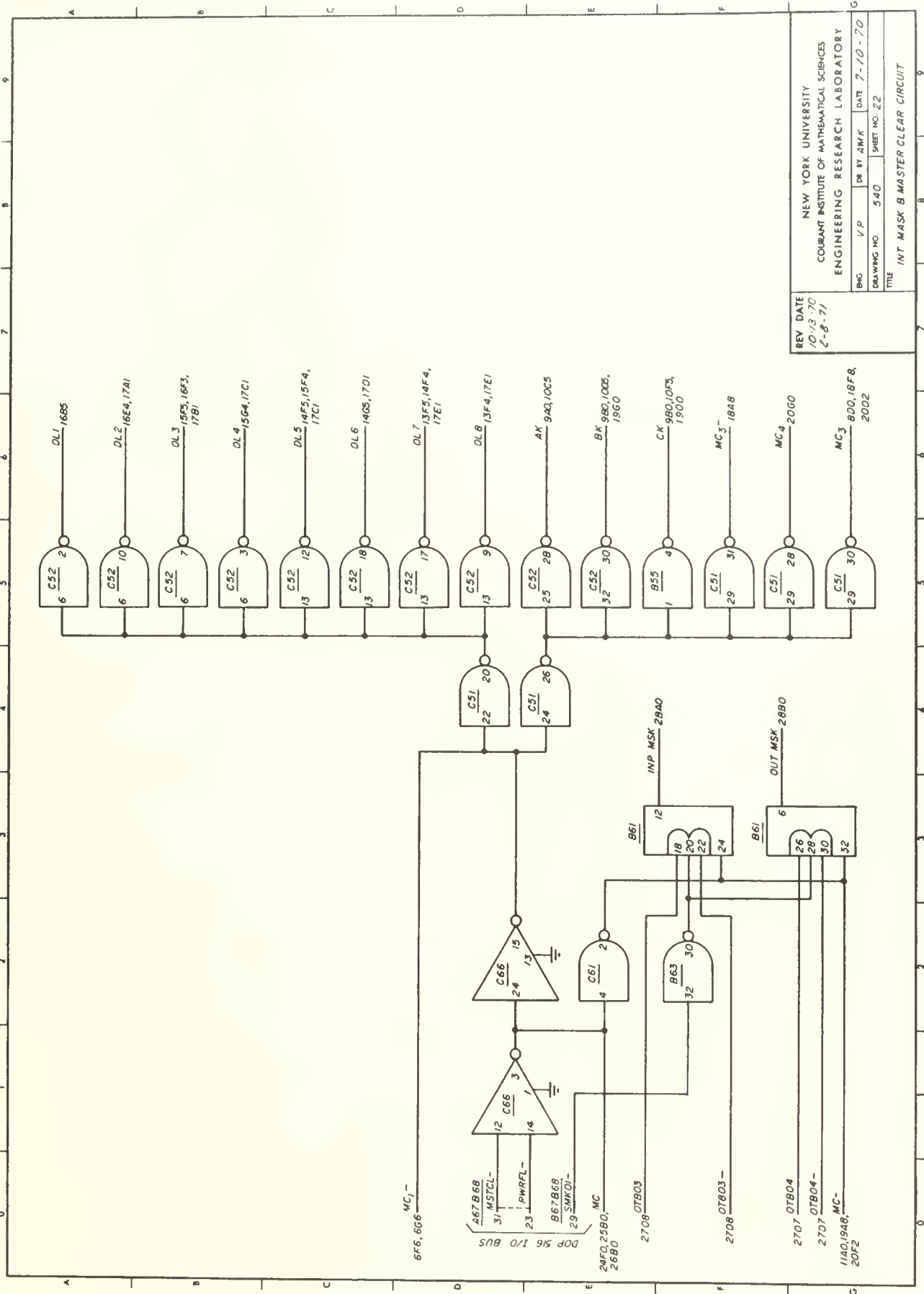| ENG | V P | DR BY A M K | DATE 7-10-70 |
| DRAWING NO | 540 | SHEET NO 23 | |

REV DATE
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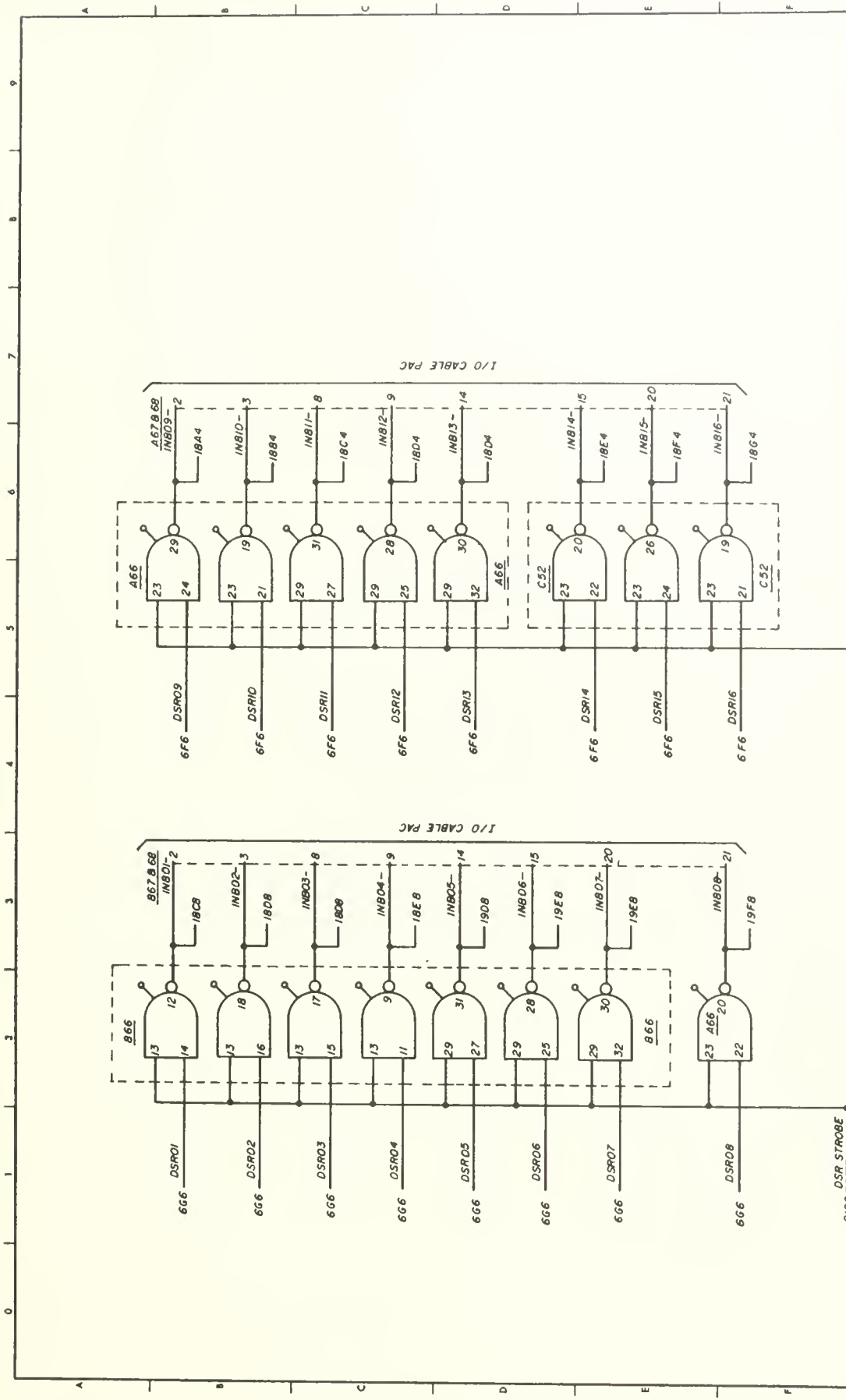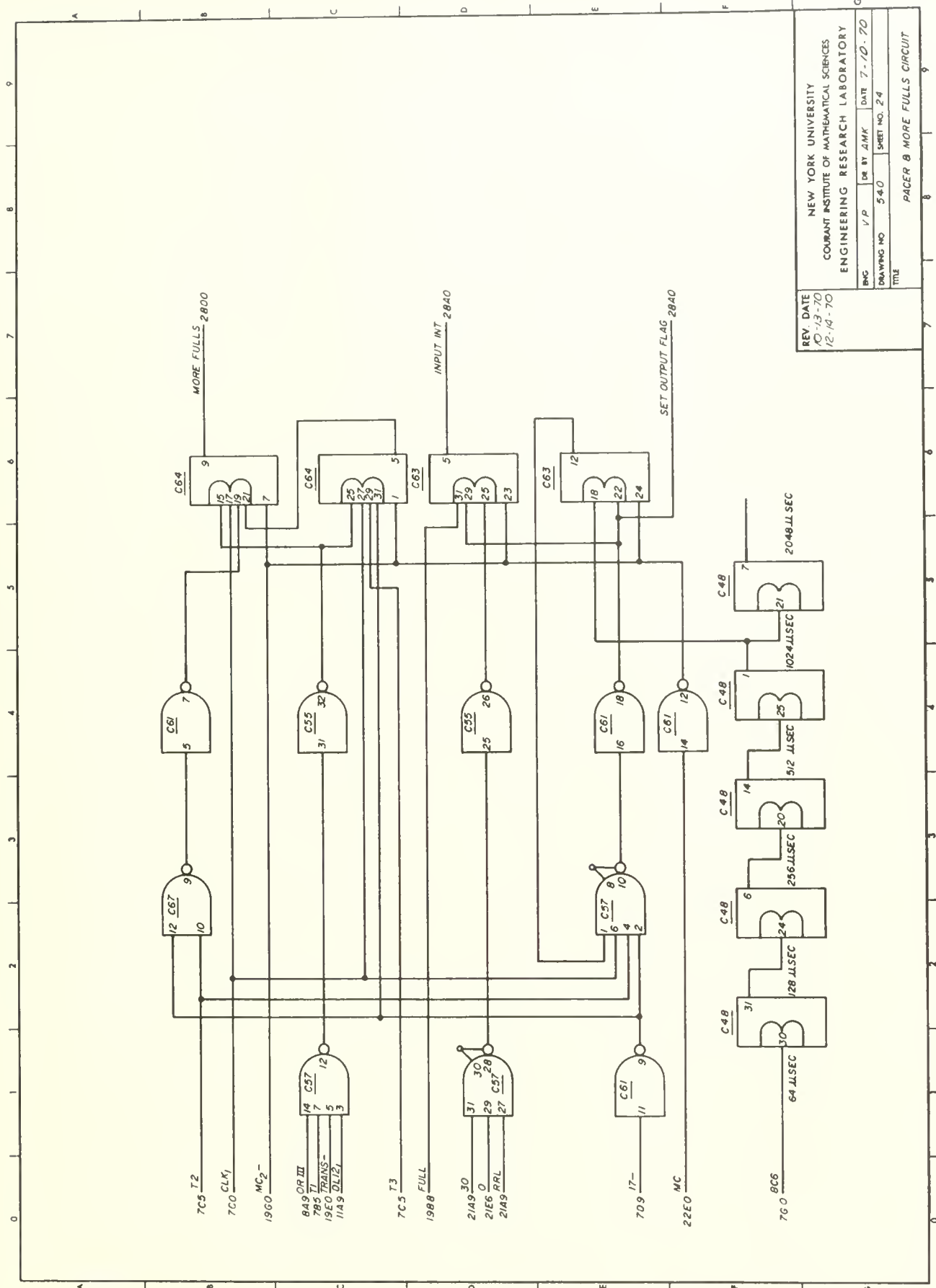Courant Institute of Mathematical Sciences
Engineering Research Laboratory

DWG	V P	DR BY AMK	DATE 7-10-70
DRAWING NO	540	SHEET NO. 24	
TITLE	PACER B MORE FULLS CIRCUIT		
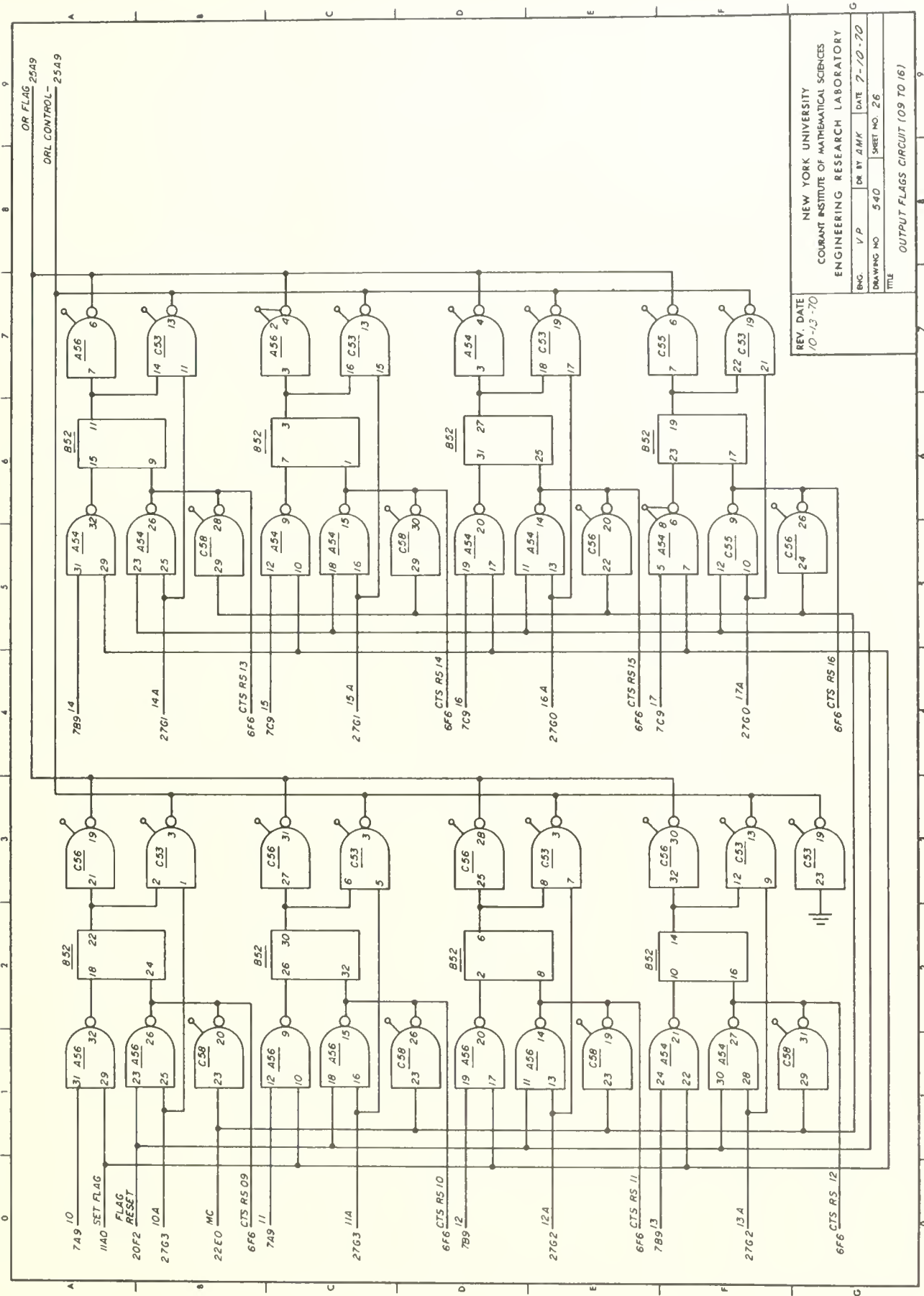
REV DATE
10-13-70
12-14-70

NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY

| ENG | V.P | DR. BY ΔMK | DATE 7-10-70 |
| DRAWING NO. 540 | | SHEET NO. 25 | |

TITLE OUTPUT FLAGS CIRCUIT (01 TO 08)

REV DATE
10-13-70

OUTPUT FLAGS CIRCUIT (09 TO 16)

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99

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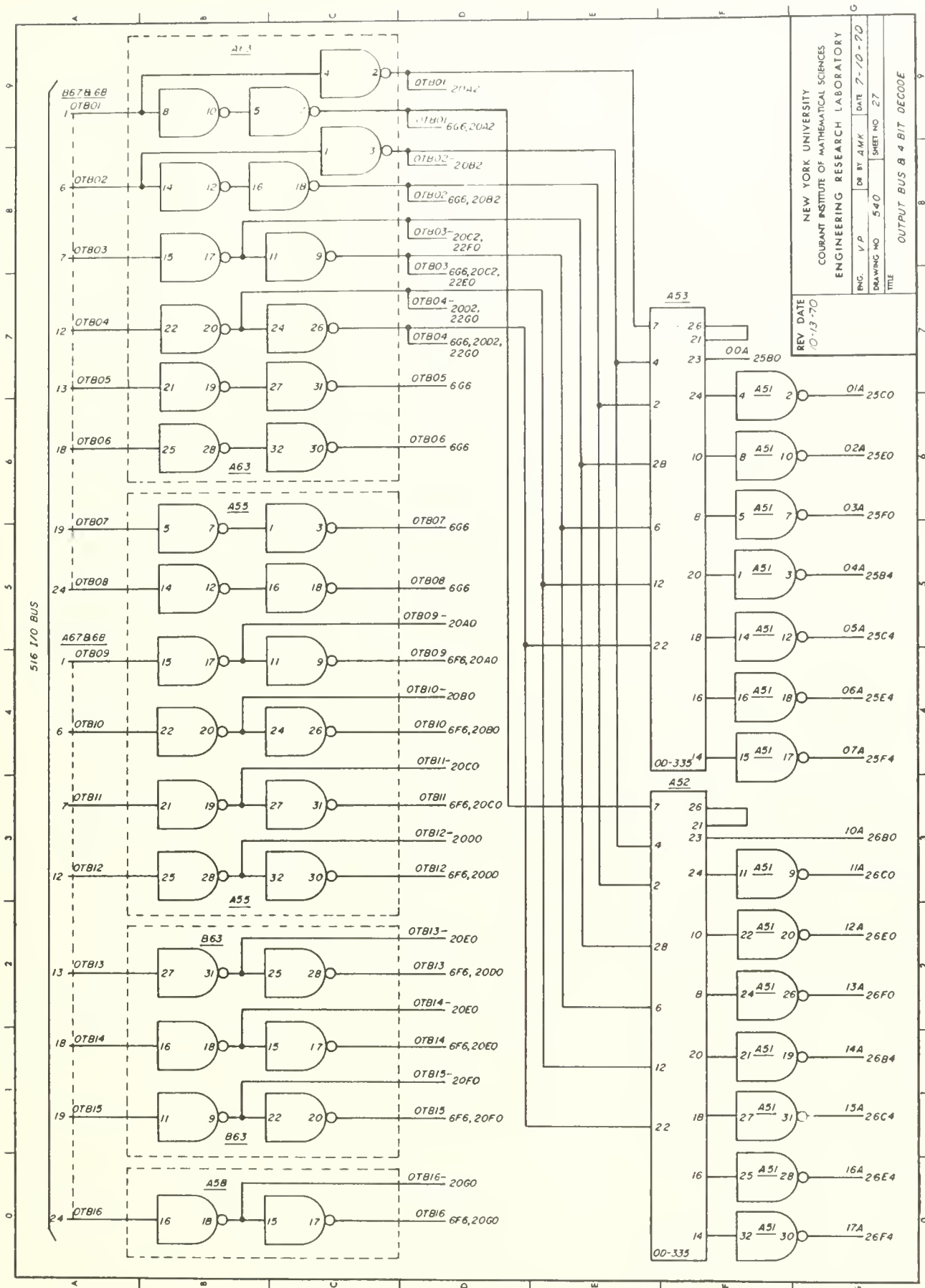ENG. V P   DR BY AMK   DATE 7-10-70
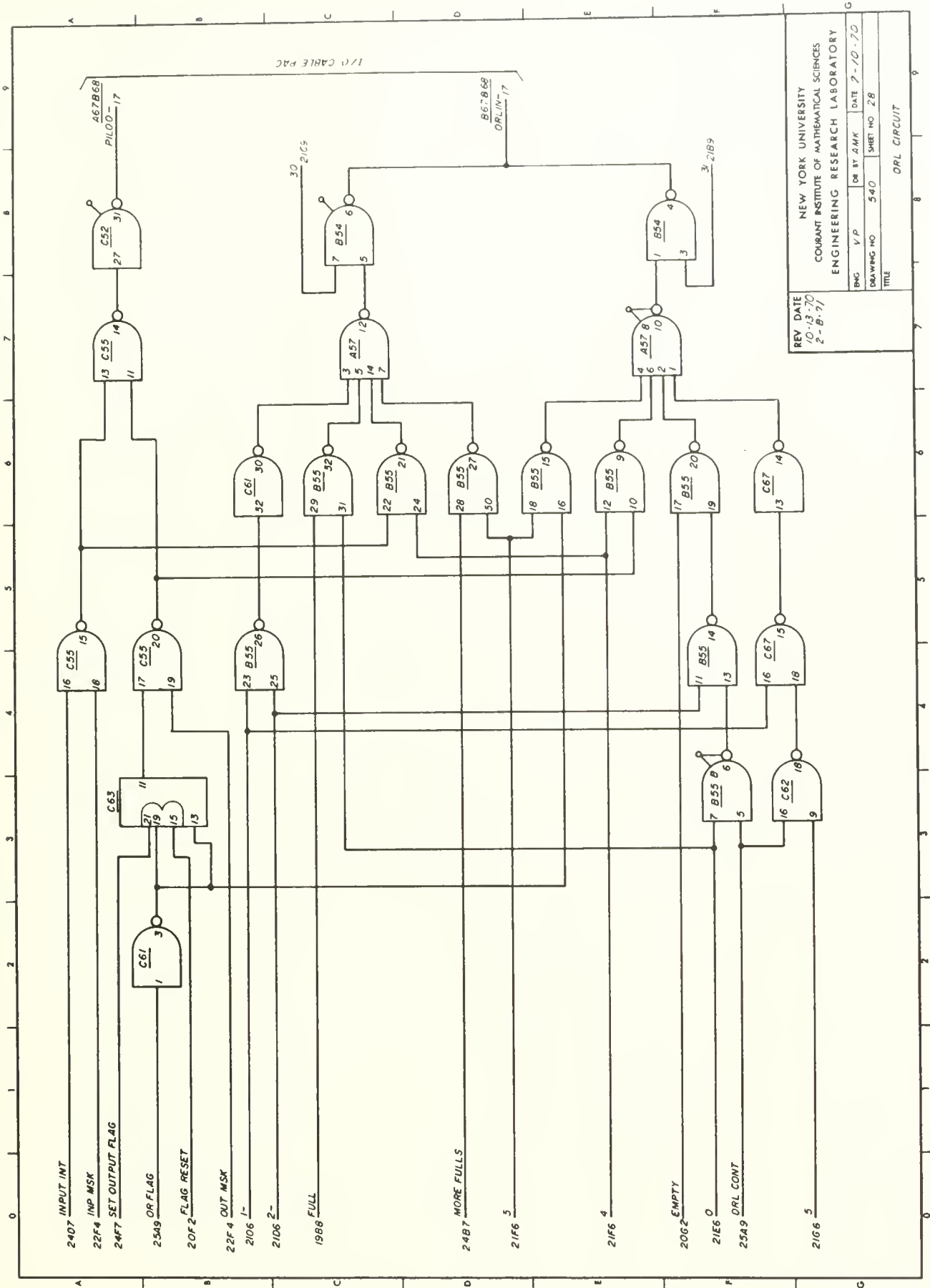DRAWING NO. 540   SHEET NO. 27
TITLE OUTPUT BUS B 4 BIT DECODE

REV DATE
10-13-70

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COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY

ENG	V P	DR BY Δ MK	DATE 7-/0-70
DRAWING NO	540		SHEET NO 29
TITLE	MULTIPLXR LAYOUT – RACK 1		

REV DATE
10-3-70

A

1
1	
2	
3	
4	
5	
6	
7	
8	

2
1	
2	DS 13-16 TO C58(PM)
3	
4	DS 9-12 TO C48(PM)
5	
6	DS 5-8 TO C38 (PM)
7	
8	DS 1-4 TO C28 (PM)

3
1	STRIP SYNC CABLE PAC
2	DG-335
3	DG-335
4	DG-335
5	
6	TG-335
7	DL-335
8	DI-335

4
1	DG-336
2	DG-336
3	
4	SM-330
5	
6	SM-330
7	DJ-335
8	

5
1	TG-335
2	OD-335
3	OD-335
4	DI-335
5	TG-335
6	DI-335
7	DL-335
8	TG-335

6
1	FA-335
2	FA-335
3	TG-335
4	FA-335
5	FA-335
6	CC-152
7	CC-154
8	I/O CABLE PAC (2)

B

1
1	
2	
3	
4	
5	
6	
7	
8	

2
1	
2	FA-335
3	FA-335
4	TG-335
5	DI-335
6	TG-335
7	OD-335
8	OD-335

3
1	
2	DL-335
3	FA-335
4	TG-335
5	DL-335
6	FA-335
7	DL-335
8	DI-335

4
1	DG-336
2	DG-336
3	
4	SM-330
5	
6	SM-330
7	
8	

5
1	DG-335
2	FF-335
3	FF-335
4	DI-335
5	DI-335
6	DI-335
7	DL-335
8	TG-335

6
1	FA-335
2	FA-335
3	TG-335
4	FA-335
5	FA-335
6	CC-152
7	CC-154
8	I/O CABLE PAC (1)

C

1
1	
2	
3	
4	
5	
6	
7	
8	

2
1	
2	PA-336
3	DL-335
4	
5	MC-335
6	8C-335
7	PA-336
8	PA-336

3
1	
2	DL-335
3	FA-335
4	DI-335
5	DL-335
6	FA-335
7	DL-335
8	DI-335

4
1	DG-336
2	DG-336
3	
4	SM-330
5	
6	SM-330
7	
8	8C-335

5
1	TG-335
2	CC-152
3	DG-335
4	PA-336
5	DI-335
6	CMO22
7	DL-335
8	CMO22

6
1	TG-335
2	DL-335
3	FA-335
4	FA-335
5	DG-335
6	PA-336
7	DI-335
8	DL-335

HUB
μ-PAC USED

8C-335	2
CC-152	3
CC-154	2
CM-022	2
DG-335	6
DG-336	6
DI-335	12
DJ-335	1
DL-335	13
FA-335	16
FF-335	2
MC-335	1
OD-335	4
PA-336	5
SM-330	6
TG-335	12
TOTAL	93

(VIEWED FROM μ-PAC SIDE)

RACK NO. 1

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ENGINEERING RESEARCH LABORATORY

ENG V P   DR BY A M K   DATE 7-10-70
DRAWING NO 540   SHEET NO 30
TITLE   MULTIPLXR LAYOUT-RACK 2

REV. DATE
10-13-70

A

1
1	D S 7&8 CABLE
2	PM 7&8 TO C32
3	X7 532A
4	X7 532A
5	X1 532A
6	X1 532A
7	PM 1&2 TO C27
8	D S 1&2 CABLE

2
1	TG-335
2	DI-335
3	TG-335
4	FA-335
5	FA-335
6	DI-335
7	DI-335
8	DG-335

3
1	TG-335
2	DI-335
3	TG-335
4	FA-335
5	FA-335
6	DI-335
7	DI-335
8	DG-335

4
1	TG-335
2	DI-335
3	TG-335
4	FA-335
5	FA-335
6	DI-335
7	DI-335
8	DG-335

5
1	TG-335
2	DI-335
3	TG-335
4	FA-335
5	FA-335
6	DI-335
7	DI-335
8	DG-335

6
1	DS 15&16 CABLE
2	PM 15&16 TO C52
3	X15 532A
4	X15 532A
5	X9 532A
6	X9 532A
7	PM 9&10 TO C47
8	DS 9&10 CABLE

B

1
1	X6 532A
2	X6 532A
3	X8 532A
4	X8 532A
5	X4 532A
6	X4 532A
7	X2 532A
8	X2 532A

2
1	DI-335
2	FA-335
3	TG-335
4	DI-335
5	FA-335
6	FA-335
7	FA-335
8	FA-335

3
1	DI-335
2	FA-335
3	TG-335
4	DI-335
5	FA-335
6	FA-335
7	FA-335
8	FA-335

4
1	DI-335
2	FA-335
3	TG-335
4	DI-335
5	FA-335
6	FA-335
7	FA-335
8	FA-335

5
1	DI-335
2	FA-335
3	TG-335
4	DI-335
5	FA-335
6	FA-335
7	FA-335
8	FA-335

6
1	X14 532A
2	X14 532A
3	X16 532A
4	X16 532A
5	X12 532A
6	X12 532A
7	X10 532A
8	X10 532A

C

1
1	DS 5&6 CABLE
2	PM 5&6 TO C37
3	X5 532A
4	X5 532A
5	X3 532A
6	X3 532A
7	PM 3&4 TO C22
8	DS 3&4 CABLE

2
1	DI-335
2	CABLE TO C17
3	"Y"LC 542Y
4	"Y"LC 542Y
5	"Y"LC 542Y
6	"Y"LC 542Y
7	CABLE TO A17
8	CABLE(HUB A28)

3
1	DI-335
2	CABLE TO A12
3	"Y"LC 542Y
4	"Y"LC 542Y
5	FA-335
6	"Y"LC 542Y
7	CABLE TO C12
8	CABLE(HUB A26)

4
1	DI-335
2	CABLE TO C67
3	"Y"LC 542Y
4	"Y"LC 542Y
5	"Y"LC 542Y
6	"Y"LC 542Y
7	CABLE TO A67
8	CABLE(HUB A24)

5
1	DI-335
2	CABLE TO A62
3	"Y"LC 542Y
4	"Y"LC 542Y
5	"Y"LC 542Y
6	"Y"LC 542Y
7	DS.13&14 CABLE TO C62
8	CABLE (HUB A22)

6
1	DS 13&14 CABLE
2	PM 13&14 TO C57
3	X13 532A
4	X13 532A
5	X11 532A
6	X11 532A
7	PM(11 & 12) TO C42
8	DS11&12 CABLE

PRE-MULTIPLXR
μ-PAC USED
PER 4 D S

DG-335	1
DI-335	6
FA-335	7
TG-335	3
"Y" LC (NYU 542Y)	4
"X" LC (NYU 532A)	8

(VIEWED FROM μ-PAC SIDE)

RACK NO 2

107

JUN 2 1971

DATE DUE

MAY 9 = 197			
MAY 1			
MAY 2 0 1971			
GAYLORD			PRINTED IN U.S.A.